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Technology Roadmap for Wide Band Gap Power Electronics 2018

第三代半导体产业技术创新战略联盟

2018年7月

Technology Roadmap for Wide Band Gap Power Electronics 2018

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Substrate, Epitaxy and Device

1.1 Background Information

The third-generation semiconductor has many attractive properties such as a large bandgap energy, high breakdown electric field, high thermal conductivity, high saturation electron velocity, and strong radiation resistance. It plays an important role in the fields of high voltage, high power, energy saving, and high efficiency, and can meet the demand of high voltage and low power consumption of electronic devices in future power system. In recent years, under the situation of the rapid development of substrate and epitaxy, the device has also achieved remarkable achievements. Some performances exceed the silicon-based devices a lot, which promotes the application and industrialization of devices represented by SiC and GaN so that it has gradually replaced silicon-based devices in some important energy fields and shown great market potential.

Since the breakthrough made by the SiC single crystal growth method in the late 1970s, especially the industrialization in the 1990s, the SiC substrate preparation technology has been in a state of rapid development, the controlling of substrate defect density and surface quality are rapidly improved, so the SiC substrate is in the upstream of the industry. However, the quality of SiC epitaxial materials and the performance and reliability of SiC-based power electronic devices is limited by substrate crystal defects and surface processing quality. In recent years, the rapid development of unipolarity device fabrication technology represented by SiC-based MOSFET has made the substrate defects more and more important to device's performance and reliability. Besides the quality of the substrate material, the cost of the substrate still occupies a relatively high proportion, which limits the rapid application of SiC-based power electronic devices. With the rapid development of downstream industries and the advancement of single crystal preparation technology, it is expected that SiC substrates will rapidly develop in the direction of large size, low crystal defect density and low cost of unit area in the next 20 to 30 years. At present, SiC-based electronic devices have been widely used in photovoltaic, power factor correction/power, automotive, wind power, and traction locomotive. The market share of SiC power electronic devices has also been rapidly developing. In 2017, Yole investigated that the market size of SiC-based power electronic devices has reached $250 million, and it is expected to reach $800 million in 2021.

While maintaining higher conversion efficiency, systems using GaN electronics can operate at higher switching frequencies, the large size and indirect cost of components such as inductors, transformers, heat sinks, drive circuits, and EMC circuits in the circuit can be effectively controlled so that we can improve the system integration and cost performance. Since the GaN substrate or SiC substrate required for GaN epitaxy is expensive, and the Si substrate has the advantages of large size and low cost, industrialization of GaN power devices on Si substrates has become a consensus in the industry.

The diamond has the advantages of high breakdown electric field, high saturation electron velocity, good chemical stability, strong radiation resistance and high thermal

conductivity, which can meet the future applications of high power, strong electric field, and extreme radiation. However, in addition to the application of diamond as a heat sink and detector, other products are still in the research stage. The diamond material epitaxy is in the upstream of the industry, and the low-cost, large-size, high-quality substrate is the basis for industrialization. In the 20th century, artificial diamond epitaxy technology developed rapidly. Based on homoepitaxial technology, a 2-inch single crystal diamond has been realized with a defect density of fewer than 1000 cm^{-2} and a 4-inch area based on heteroepitaxial growth. However, homoepitaxial growth depends on the quality and size of the substrate, and heteroepitaxial nucleation and defect control are difficult, which severely limits the development of diamond. The doping of diamond is very difficult, and it is hard to form high conductivity at room temperature. At present, termination of diamond surfaces with hydrogendevices with P-type surface conductivity at room temperature have emerged in high-voltage, high-temperature high-frequency device applications. However, the hydrogen terminal diamond surface conductance has the disadvantages of low carrier mobility and poor stability of the device. In general, diamond substrates are expected to develop rapidly in the future 20 to 30 years toward large size, low crystalline defect density, and low unit cost. With the improvement of epitaxial quality and carrier mobility, as well as breakthroughs in key issues such as new doping technology, the characteristics of diamond electronic devices are expected to surpass existing GaN, SiC-based electronic devices, and diamond-based electronic devices will get a certain market share in the power, automotive, wind power, and traction locomotive industries.

As a new type of ultra-wide bandgap semiconductor material, gallium oxide (Ga_2O_3) has received extensive attention. Compared with SiC and GaN, Ga_2O_3 is a wide bandgap material with a bandgap of ~4.9 eV, and its critical breakdown electric field is 8MV/cm, which is suitable for making large voltage and high power field effect transistor. Due to the strong electric field breakdown resistance, Ga_2O_3-based electronics can achieve low heat losses by reducing the on-resistance. Although Ga_2O_3 has lower electron mobility than SiC and GaN, it can withstand the high electric field required to reach a saturated electron rate due to its higher breakdown electric field, also, it has high power frequency product, and the Johnson quality factor is higher than SiC and GaN. Therefore, Ga_2O_3-based electronic devices are not only suitable for power switching devices, but also for RF devices. In addition, the most attractive advantage of Ga_2O_3materials is that its single crystal is easy to prepare, such as Czochralski method, floating-zone technique, vertical Bridgman method, guided-mode method, so it is possible to realize the cost-effective thin-film epitaxy, which facilitates the realization of inexpensive, high-performance electronic devices. Since the Ga_2O_3material device is used for high power and high withstand voltage applications, the crystal quality is highly demanded. Correspondingly, most of the devices for Ga_2O_3 are β- Ga_2O_3 single crystal. At present, the preparation of Ga_2O_3 materials and devices is still in infancy. The factors include larger device series resistance and lower electron mobility, which restricts Ga_2O_3 devices, especially MOSFET devices. To utilize the ultra-wide bandgap of Ga_2O_3, it is necessary to

continue to optimize and improve the quality of single crystal and epitaxy, device structure and process flow.

This roadmap describes the development trends of SiC substrates and epitaxy, SiC power devices, GaN epitaxial and power devices, diamond materials and devices, Ga_2O_3 epitaxy and devices in the next 30 years (2018~2048). We will discuss the key aspects of substrate diameter, crystal defect density, and unit area cost, the key index of SiC, GaN, diamond, Ga_2O_3 such as electrical properties, packaging, heat dissipation, reliability, and the cost.

1.2 Summary of the driving force of the development of technology / product

Market: With the continuous drive of the downstream market of the power system for the high voltage and low power consumption of power electronic devices, the third generation of power electronic devices represented by SiC and GaN will gradually replace Si-based power electronic devices in some fields. Therefore, the market share will be increasing year by year, which also drives the growth of substrate and epitaxy. Commercial products appear in diamond power electronic devices as well.

Cost: As an alternative product of Si-based devices, SiC and GaN devices are challenged by the cost in the process of marketization. The continuous reduction of cost is their own development trend and market demand. The increase of artificial diamond wafer size will greatly reduce its material and device costs.

Material defect density: Due to the demand for system reliability, the requirements for device performance and reliability will become more and more stringent, so higher requirements are placed on the defect density of substrate and epitaxial materials.

Voltage/current carrying capacity: With the high power and high-efficiency requirements of the power electronic system, the demand for voltage/current carrying capacity of SiC power devices and GaN power devices is increasing. The development of diamond power devices is also driving the increase of device voltage/current carrying capacity.

Packaging and heat dissipation: SiC power devices, GaN power devices have low loss, and the operating junction temperature range is higher than that of Si devices, so the cooling device volume can be reduced. These excellent features promote the development of power devices toward integration, miniaturization, and high efficiency.

Frequency requirements: SiC power devices and GaN power devices have high electron saturated drift rates and small capacitance, so the device operating frequency can reach above MHz, thus reducing the passive device and the overall size of the system.

Conversion efficiency: The increase of power conversion efficiency in large-scale power consumption not only saves energy consumption but also reduces the need for

heat dissipation. The extremely high thermal conductivity of diamond is beneficial to reduce power consumption and improve conversion efficiency.

Reliability: The superior characteristics of high temperature, high frequency, high power and anti-irradiation of SiC power devices and GaN power devices make it more likely to be used in future high-end industrial fields and extreme environments. Improvement of the reliability of the third-generation semiconductor promotes its market expansion.

1.3 Key Performance/Development Trend of Parameter

1.3.1 SiC substrate and epitaxy

1.3.1.1 SiC substrate

- **Substrate diameter**

➢ Development trend: (as shown in Fig1.1)

- The diameter of the substrate currently used is mainly 100mm. With the gradual popularization and application of SiC-based power electronic devices, the cost of the device is becoming more and more sensitive. Large-diameter substrates can effectively reduce the cost of device fabrication. For example, using a substrate with a diameter of 150 mm can reduce the device fabrication cost by about 30% compared to a diameter of 100 mm. Therefore, It is expected that the proportion of large-sized substrates will continue to increase in the next 30 years..
- At present, the mainstream manufacturers have completed the research and development of 150mm diameter SiC substrate and have entered the mass production stage. Therefore, from 2018, the proportion of 100mm diameter SiC substrate will start to decrease year by year.
- Some manufacturers have completed the research and development of 200mm diameter SiC substrate and can provide a small number of samples. It is estimated that the 200mm diameter substrate will enter the market before 2020.

➢ Challenge:

- Temperature field design and implementation:
  The suitable temperature field is the basis for the preparation of SiC single crystal. The quality of the single crystal is directly related to the temperature field. Unsuitable temperature field is likely to cause cracking

of single crystal and the proliferation of crystal defects. With the increase of the diameter of the single crystal, the size of the hot zone increases rapidly, which makes the design and the implementation of the suitable temperature field difficult.

- Low defect density seed crystal:
  It is difficult to expand the diameter of the single crystal by the vapor-phase growth method. Besides, it is hard to obtain low defect density seed crystal by using small diameter seed crystal diameter expansion.
- Comprehensive control of large-size single crystal and crystal defects:
  The increase in the size of single crystals tends to be accompanied by a decrease in the quality of the crystal. How to increase the size while taking into account the control of the density of crystal defects is another key problem that needs to be solved to increase the size of the substrate.

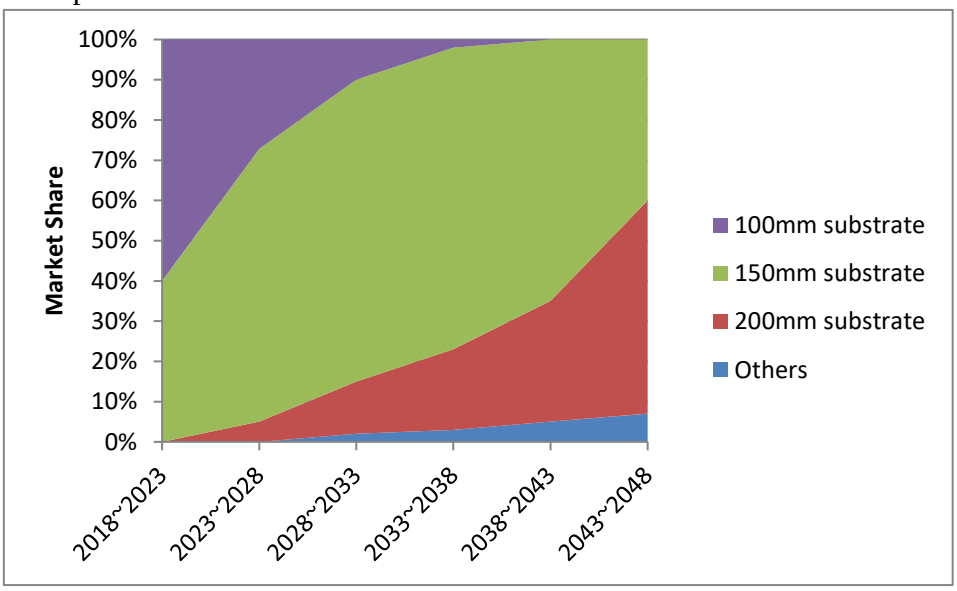


Fig 1.1 The development trend of SiC substrate size

➢ Potential solution:

- Using numerical simulation to guide the design of large-scale temperature field of single crystal growth, to achieve temperature field control in different growth stages.

■ **Crystallographic defect density**

➢ Development trend: (as shown in Fig1.2)

- With the rapid application of SiC-based power electronic devices, the requirements for device performance and reliability are getting more and more stringent. Crystal defects (such as microtubules, threading screw dislocations (TSD), and basal plane dislocations (BPD)) can adversely affect the device. With the rapid development of diverse technology that decreases and converts single crystal defects, it is expected that the density of crystal defects in the substrate will continue to decrease.
- At present, mainstream manufacturers have the ability to fabricate low

micro tube density substrates (<1/cm2). The reduction of TSD and BPD density will become the focus of substrate manufacturers' research and development work. Therefore, the density of TSD and BPD in substrates is expected to decrease.

➢ Challenge:

- Cost:

  In order to reduce the density of crystal defects, the conventional process conditions can no longer satisfy the growth of single crystals with low crystal defect density, so it is necessary to introduce a new process and increase the complexity of the process, which will push up the cost of the single crystal.

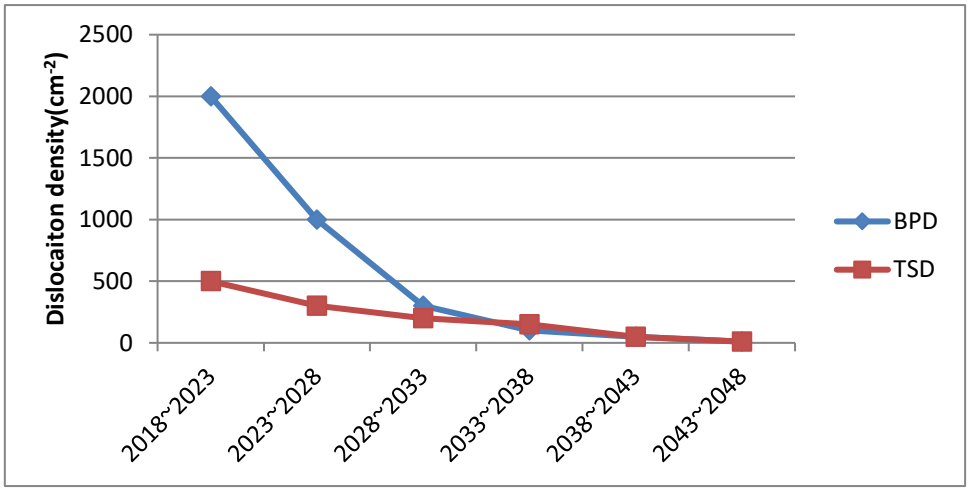


Fig 1.2 The development trend of dislocation density(TSD, BPD) of the substrate

■ The unit area price of substrate:

➢ Development trend: (as shown in fig1.3)

- The cost per unit area of the substrate will decrease as the proportion of large-diameter substrates continues to increase.
- Taking a single crystal of 150 mm diameter and a single crystal of 100 mm diameter as an example, the total growth cost of the former is about 1.5-2 times that of the latter.
- The available thickness of single crystals is increasing. Taking a 100mm diameter single crystal as an example, the average available thickness of single crystals prepared by most single crystal manufacturers is about 15mm before 2015, which has reached 20mm by the end of 2017. It is expected that the average usable thickness of single crystal will continue to increase, which will continuously reduce the unit area cost of the substrate.
- As the defect density of the substrate crystal decreases, the process complexity increases, and the rate of finished products decreases in a short period of time, which will push up the substrate price.
- Based on the above points, in the recent 5 years, the unit area price of the

substrate will decrease slightly for the rapid promotion of the 150mm diameter substrate. After the most substrate manufacturers have completed the research and development of the single crystal growth of low dislocation and the thick single crystal growth, the unit area price of the substrate will reduce rapidly.

- Challenge:
  - The research and development cycle of the single crystal growth of low dislocation
  - For the growth temperature of SiC is high, traditional methods for reducing defects (such as masking method) are no longer applicable, so it is necessary to invest in a long time and a large cost to develop new processes, and a long research and development cycle may hinder the unit area cost reduction of the substrate.
  - With the increase of the thickness of single crystal growth, the residual internal stress of single crystal increases rapidly, which may lead to the degradation of single crystal quality and even the cracking of single crystal. It is difficult to not only increase the available thickness of single crystal but also improve the quality of single crystal.

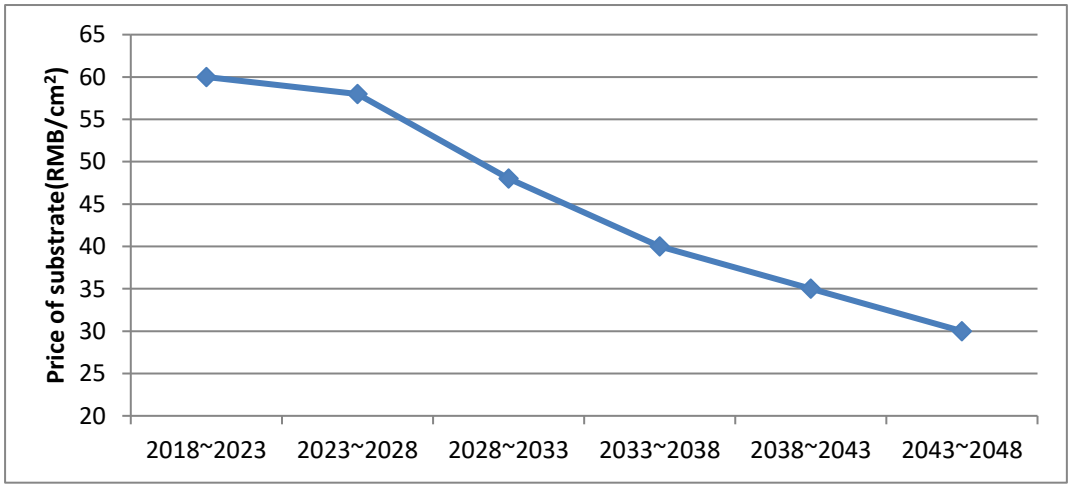


Fig 1.3 The development trend of per unit price of the SiC substrate(RMB/cm^2)

1.3.1.2 SiC epitaxy

- **Size:**
- Development trend
  - Diameters of SiC with 100mm and 150mm are the normal sizes of SiC epitaxial wafers. With the widespread use of SiC devices, the cost requirements for SiC devices are becoming more and more stringent. Larger SiC epitaxy can effectively reduce the cost of subsequent device fabrication, so in the next 30 years, the proportion of large-size SiC epitaxial wafers will increase year by year.
  - Now, mainstream substrate suppliers at home and abroad are already

selling 150mm diameter SiC substrates or have completed 150mm substrate preparation technology. The market share of 100mm diameter substrates will decrease year by year.

- At present, the main manufacturers of SiC devices in China still use 100mm SiC epitaxial wafers widely. Under the condition that the supply of 150mm SiC substrate cannot be greatly improved, it is expected that 100mm SiC epitaxial wafers will be widely used in the next three years.
- The international mainstream SiC device manufacturers have basically completed the transfer to 150mm SiC technology. The demand will grow rapidly in the next 5-10 years. Some companies' original process lines also retain 100mm technology.
- Although the 200mm SiC substrate and epitaxy have been demonstrated, it will be a long process entering the SiC power device market. After 5 years, 200mm SiC epitaxial technology will be mature, and 200mm SiC power device production line may appear after 10 years.

➢ Challenge:

- Cost: By now, 100mm SiC epitaxial wafer is close to its lowest price, and the price reduction space is limited in the future; the price of 150mm SiC epitaxial wafer is still relatively high due to insufficient substrate supply. As the substrate quality improve and wafer supply increase and the yield of epitaxial wafers increases, the price of the epitaxial wafer will reduce rapidly.
- Control of epitaxial wafer uniformity: The increase of epitaxial wafer size tends to be accompanied by the decline of epitaxial wafer uniformity. How to control the uniformity of the large-scale epitaxial wafer is a key problem to be solved to improve device yield and reliability and thus reduce cost.
- Epitaxial defect control: Large-sized devices are the mainstream demand in the future application market. Defect density is the key index to restricting the yield of large-size chips. Therefore, epitaxial defect control including crystal defects and surface topography defects is a major challenge.

➢ Potential solution:

- Improve the temperature field and flow field distribution of large-scale epitaxial growth, and control the interface morphology at the initial stage of epitaxy.

■ BPD dislocation density

➢ Development trend (as shown in Fig 1.4)

- The basal plane dislocation (BPD) is an important crystalline defect affecting the stability of SiC bipolar power devices. Continuous reduction of BPD density is the main direction of epitaxial growth technology. As the substrate quality is improved, the BPD of SiC epitaxial layer is expected to reduce from $1/cm^2$ to $0.1/cm^2$.

- The most mature preparation technology of SiC crystal is physical vapor transport (PVT). At present, the SiC crystal grown by PVT has a high BPD density, and the BPD which is harmful to the device in the epitaxial layer mostly comes from the BPD in the substrate. Therefore, improving the crystal quality of the substrate can effectively reduce the BPD dislocation density of the epitaxial layer.
- With the application of SiC devices, the device size and flow capacity are increasing, and the requirement for crystal defect density is stringent, so the crystal defects density of SiC epitaxial wafers will decrease.

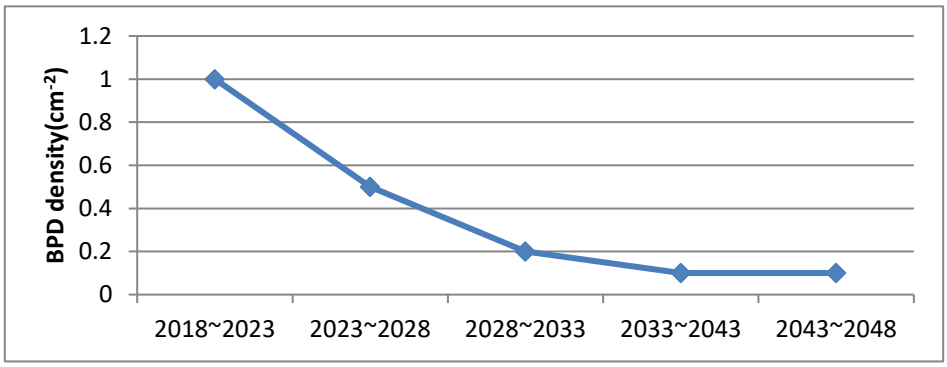


Fig 1.4 The development trend of BPD density in SiC epitaxial wafer

■ **The thickness of the epitaxial wafer**

➢ Development trend

- The application advantages of SiC are high-voltage, ultra-high voltage devices. At present, 600V, 1200V, 1700V SiC devices have been commercialized. It is expected that the application requirements of 3300V and 6500V, and even more than 10,000 volts will be rapidly improved in the future, and then the SiC thick epitaxial wafers will be needed.
- In order to obtain thick epitaxial wafers, fast epitaxial growth technology will become the mainstream of technology development.

➢ Challenge

- Device stability: especially the stability of bipolar SiC power devices. Due to the existence of BPD dislocations in the epitaxial layer, under the forward bias condition, the stacking fault defects caused by the BPD will expand, leading to reduce carrier lifetime and drift in forward voltage.
- Carrier lifetime: The current carrier lifetime of 100μm thick SiC epitaxial layer is 1-2 μs, which cannot fully meet the manufacturing requirements of high-performance SiC power devices, so it needs to improve carrier lifetime.

➢ Potential solution

- Optimize the growth process and improve the conversion efficiency of BPD dislocation to TED dislocation in epitaxial growth.
- Use the method of enhancing the carrier lifetime of the epitaxial layer, such as high-temperature oxidation and annealing processes, to improve carrier lifetime.

■ **The price of a unit area of epitaxial wafers**

➢ Development trend (as shown in Fig1.5, Fig1.6)

- The substrate accounts for more than 50% of the cost of the epitaxial wafers. As the price of the substrate decreases and equipment, factory, and labor costs will reduce as the equipment improves, the epitaxial price will decrease. As the epitaxial quality requirements become more and more stringent, the cost of research and development and yield loss will remain at about 7%.
- In the recent 5 years, the price of unit area will be reduced slightly with the rapid promotion of 150 mm diameter substrate. With the price reduction of equipment, factory, and labor, the price reduction of a unit area of epitaxial wafers will be relatively fast.

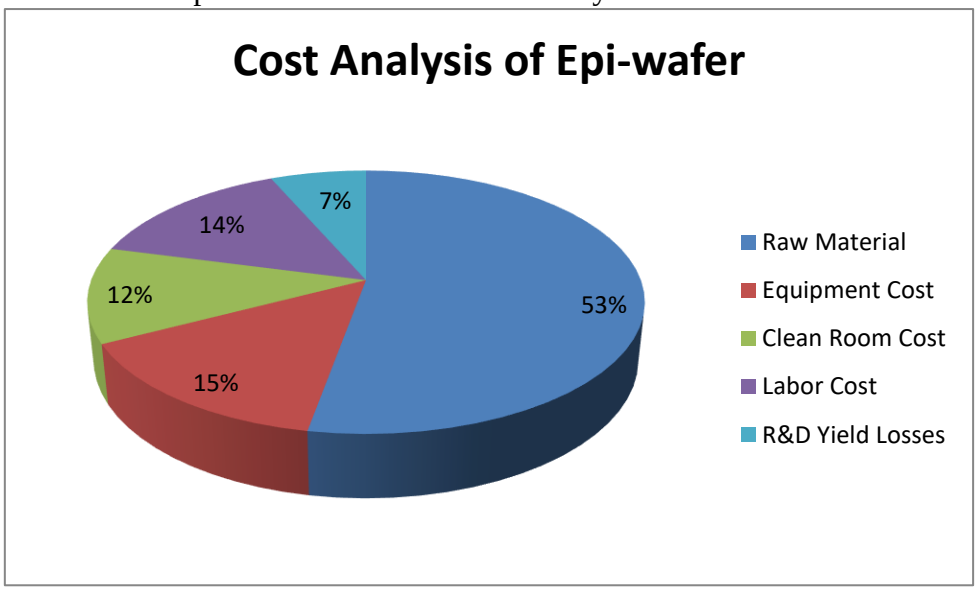


Fig 1.5 Cost analysis of epitaxial wafers

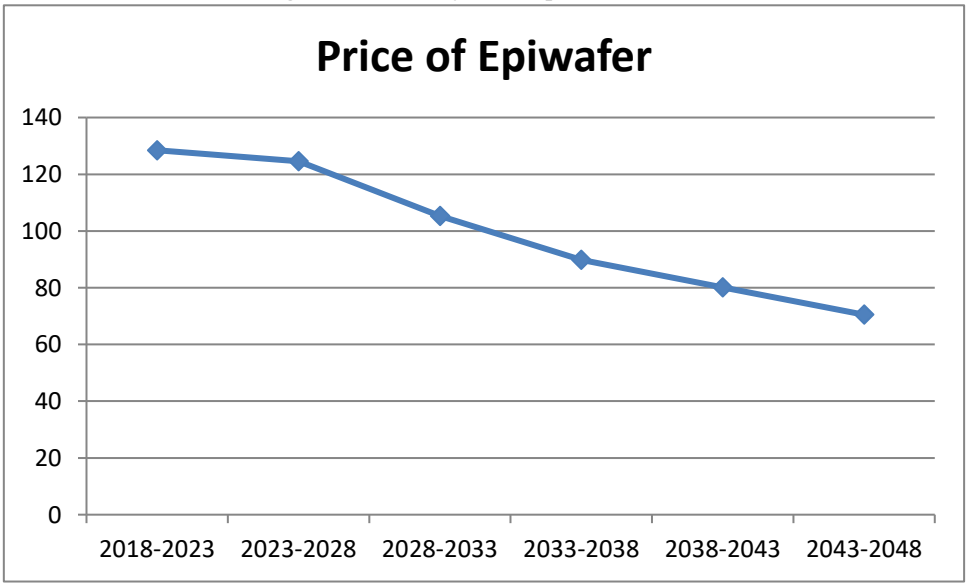


Fig 1.6 The development trend of a unit price of the SiCsubstrate(RMB/cm^2)

1.3.2 SiC power device

1.3.2.1 Structure and size

- **SiC Schottky device**

➢ Development trend: (as shown in Fig1.7[1], Fig1.8[2])

- SiC Schottky devices are widely used in power factor correction (PFC) circuits, which are the most important application areas for SiC devices, with a share of more than 50%. By now, SiC devices mainly include pure Schottky-contacted SBD devices and junction-barrier JBS devices with p-type implants. The former is widely used in the low-voltage field, and the latter is used in high-voltage applications. To meet the demand of surge resistance, SiC Schottky device of JBS type is often used for power conversion circuits.
- The reverse recovery loss of SiC Schottky devices does not change with temperature and forward current, so it can achieve fast recovery regardless of the environment. Junction capacitance is the main indicator affecting its charge and discharge loss, so the next step should be developing low-capacitance SiC Schottky devices.
- The specific on-resistance of SiC Schottky devices has been reduced to $1m\Omega.cm^2$, and the forward voltage drop has been greatly improved. In order to obtain a SiC Schottky device of lower conduction voltage drop, a trench structure can be used to increase the effective Schottky contact area or reduce the carrier conduction path (thinning the substrate).
- To enhance the device reliability， packaging working under high temperature is an important way to improve the efficient operation of SiC Schottky devices. A part of the failure of SiC Schottky devices is due to the mismatch of thermal expansion coefficients of the packaging materials leading to the premature damage of the device. Therefore, optimizing the device current sharing capability, improving packaging technology is the future development trend.

➢ Challenge

- Cost: As the area of SiC Schottky device chips continues to decrease, reducing the cost of the device in the development process is an important challenge.
- Low forward voltage drop Schottky devices: As the static operating capability increases, the on-resistance of the device must be reduced, so it is necessary to obtain SiC devices with low dropout Schottky contact and good wafer uniformity.
- Low reverse leakage Schottky device, the edge termination can effectively improve the breakdown characteristics and reduce the reverse leakage current, so that the breakdown voltage of the device is more than 80% of

the ideal planar junction breakdown voltage.

- High temperature operation: to improve the carrier drive capability of the device, to optimize the internal heat balance of the cell, to improve the heat dissipation capability of the device, to optimize the ohmic contact reliability design of the device, and to improve the high temperature resistance of the device.

➢ Potential solution

- Optimize the internal cell layout and structure of the device with a new terminal structure design.
- Optimize the balance of the forward conduction resistance and reverse breakdown of the devices using a low dropout Schottky contact design or trench structure design.
- Improve the high-temperature reliability of ohmic contact of the device.

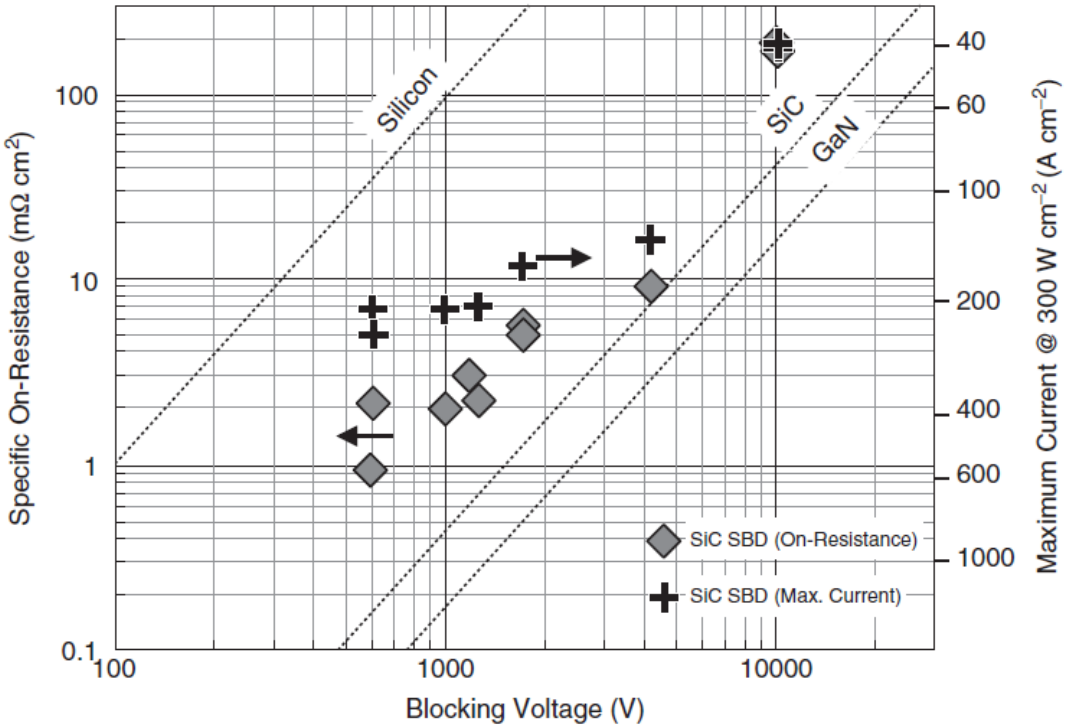


Fig 1.7 The development of SiC Schottky device

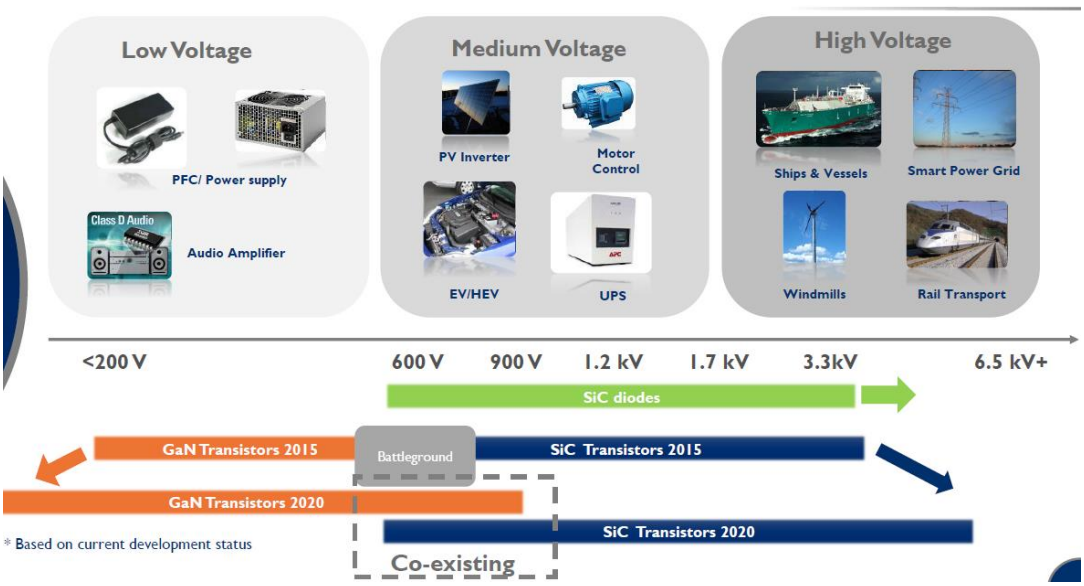


Fig 1.8 The distribution of withstand voltage of SiC Schottky device

■ **SiC MOSFET device**

➢ Development trend: (as shown in Fig1.9[3], Fig1.10)

- The current mainstream SiC three-terminal device is MOSFET device. The MOSFET is based on the control of the gate terminal to implement turning on and turning off of the switching device, so as to meet the requirements of high frequency and high power. It can replace the conventional Si-based IGBT device in some fields, and the device performance does not drift severely with operating temperature changes. The on-resistance of the MOSFET has a positive temperature coefficient, and the device performance does not drift severely with the change of the operating temperature, so MOSFET is suitable for parallel operation.
- The specific on-resistance of SiC MOSFETs can be reduced to 1mΩ.cm2. The withstand voltage is mainly distributed in the medium voltage field. SiC DMOSFET devices are used in more than 10kV. The chip area is more than 8×8mm2 and is developing to 6 inches.
- SiC UMOSFET has lower specific on-resistance than DMOSFET and has better performance. The channel mobility of SiC non-polar plane is high, and the channel structure MOSFET has higher cell integration. Therefore, SiC UMOSFET become the focus of R&D and application in the medium voltage field.
- SiC MOSFET devices with integrated Schottky devices improve the device's third quadrant operation while reducing overall chip area, increasing device integration and reducing cost.
- A SiC MOSFET device with an accumulated channel enhances the forward conduction capability of the device and develops in large the crystal size.
- SiC MOSFET devices have characteristics of high-temperature and high frequency-operation, but the high-temperature working potential of SiC

MOSFET device is not exerted due to the mismatch between the thermal expansion coefficients of SiC and SiC chip's lead and the limitations of packaging materials and technologies. Selecting materials with excellent insulation properties and high thermal conductivity as device packages can effectively avoid thermal stress caused by temperature changes, which is an important point for future SiC power device packaging technology.

- Challenge:
  - The SiC material can form an oxide layer by in-situ oxidation as a gate dielectric layer, which has a high compatibility with the process of Si. However, the process of SiC oxidation is much more complicated than Si oxidation. Besides, high-density interface defects and interface trap charges have a huge influence on carrier transport and recombination in the interface channel of SiC-based MOSFETs, resulting in carrier loss and device mobility degradation.
  - The gate dielectric of SiC MOSFET will change under high-temperature conditions, causing the threshold voltage of the device to be unstable, and the interface defect causes the gate leakage current of the device to rise.
  - The gate voltage driving of SiC MOSFET is different from that of Si device. The former has asymmetry, usually +20V/-10V, so we should pay special attention to the driver circuit design of SiC MOSFET device.
  - The breakdown electric field of SiC is high, so that the electric field in the gate dielectric SiO2 is also strong in reverse operation, especially in the trench MOSFET structure, the two-dimensional electric field concentration of the groove angle reduces the stability of the device.
  - We can expand the capacity and reduce the cost of the device through improving wafer yield control of SiC MOSFET, the on-chip and inter-chip consistency of the device.
  - Improvement of the high-temperature and high-frequency reliability of ohmic contact of devices.

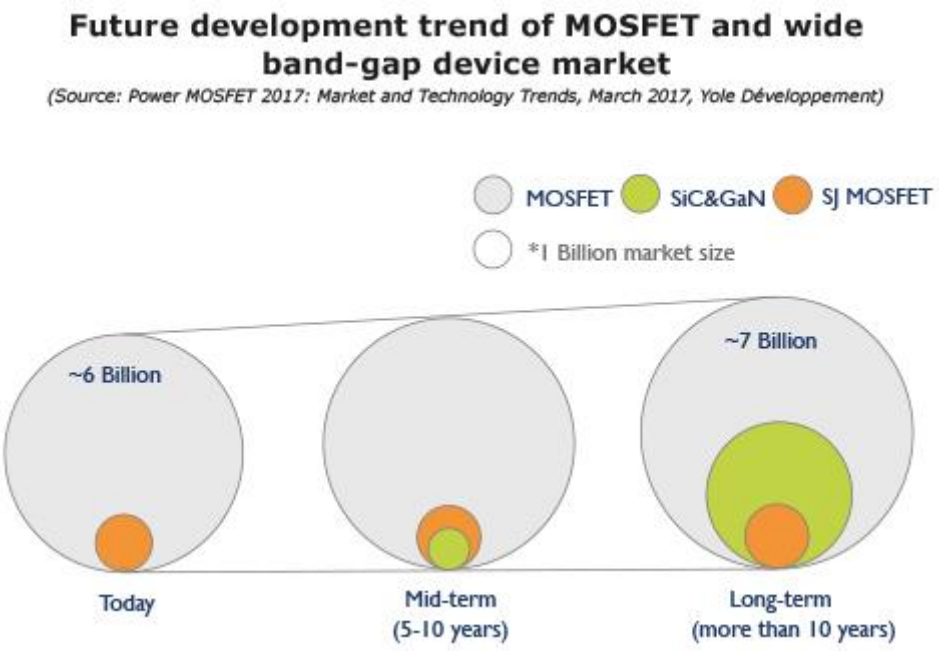


Fig 1.9 Market share analysis of SiC MOSFET device

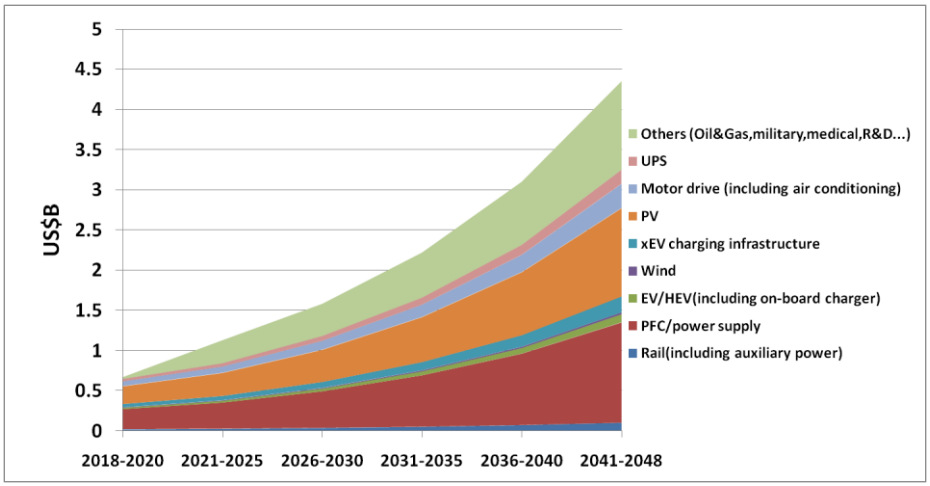


Fig 1.10 Market distribution of SiC MOSFET device in the future

1.3.2.2 Electrical properties

- **SiC Schottky device**

➢ Development trend of the device: (as shown in Fig1.11)

- The structure of SiC junction barrier Schottky devices with p-type implants will become more and more to meeting high power requirements and improving the surge resistance of devices.
- Cell design: including the effect of the integrated cell on chip current density, heat distribution uniformity, breakdown point consistency and chip capacitance. Common SiC Schottky diode cell topological layouts

include strip distribution, square lattice distribution, spherical lattice distribution, etc. Among them, strip cell design is a relatively mature technical means.

- Junction termination extension (JTE), field plate (FP), etched mesas, and combinations of them are used to reduce the reverse leakage current characteristics of the device.

➢ Challenge:

- It's a contradiction between the blocking voltage and the on-resistance of the power device. Therefore, we need through optimization of the structure to design SiC Schottky diode with high blocking voltage and low forward voltage drop.

➢ Potential solution:

- A SiC Schottky device with a minimum on-conduction voltage drop and good reverse blocking characteristics can be obtained by simulation using a trench-type structure, a double-barrier metal contact, etc., in combination with the process difficulty and repeatability.

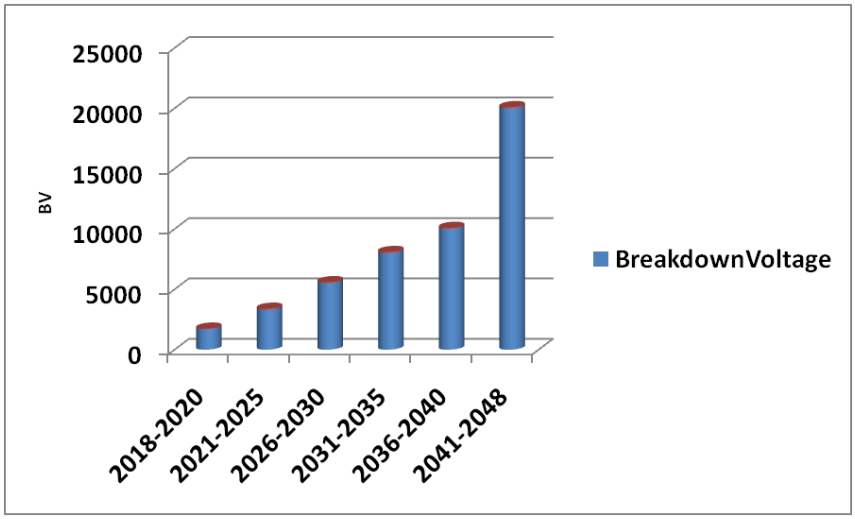


Fig1.11 The blocking voltage of SiC Schottky device

➢ Development trend of reliability:

- An important reliability issue for SiC Schottky devices is the reverse bias leakage current of the device.
- The conduction characteristics and reliability of SiC SBD devices and JBS devices are well guaranteed after repeated surge current surges.
- After high temperature and high-frequency operation, the electrical properties of the device did not drift seriously.

➢ Challenge:

- How to optimize the SiC Schottky device of higher performance, improve the forward conduction and reverse blocking capability, ensure high temperature and high-frequency reliability.

- Potential solution:
  - JBS diodes are less affected by thermal induced voltage surges and have a higher reliability of thermal induced surge voltage.
  - For SiC SBD devices and JBS devices, reducing the self-heating effect of devices and their impact on high voltage reliability is an important research and development direction.
  - To optimize device structure and package form to reduce thermal resistanceas the device can work at low temperatures.

■ **SiC MOSFET device:**

- Development trend of the device: (as shown in Fig1.12[4], Fig1.13)
  - The development of SiC MOSFET device structure is similar to that of Si devices. DMOSFET devices are the most mature SiC MOS devices at present. The electrical properties of the devices are more stable, and the gate oxide is effectively protected by the good shielding layer. The typical cell size of SiC DMOSFET devices is 10μm. The device cell structure is mostly strip-type cells, and other cell layouts such as rectangular cells, square cells, diamond cells, etc.
  - Optimize device structure, reduce JFET resistance, drift region resistance, channel resistance, substrate resistance, etc., thereby improving the on-state characteristics of the device.
  - Junction termination extension (JTE), field plate (FP), etched mesas, and combinations of them are used to optimize the device termination structure and improve the breakdown characteristics of the device.
  - Optimize device cell layout and interlayer structure, reduce the gate capacitance of the device so that to improve the dynamic characteristics of the device
  - The cell gate integration can be further improved by using a trench gate structure to form SiC UMOSFET. The typical cell gap of SiC UMOSFET is 5 μm.
  - The new structure is used to reduce the gate dielectric field of the SiC UMOSFET and improve the reverse blocking reliability of the device.
  - Optimize the design of the gate dielectric structure of SiC MOS devices, reduce device gate-drain capacitance, gate-source capacitance, etc., which can effectively improve the dynamic switching performance of the device.
- Challenge
  - How to get high-quality SiC MOS gate dielectric structure, improve the forward turn-on gate bias and reverse turn-off gate bias capability of SiC MOSFET devices is a major problem.
  - How to optimize the device channel layout, improve device channel mobility, and thus reduce channel resistance.
  - How to reduce the gate capacitance of the device is an important project to improve the high-frequency switching capability of SiC MOSFET devices.
  - How to effectively protect the trench gate dielectric of SiC UMOSFET.

- Potential solution
  - SiC MOS gate dielectric can use traditional SiO_2 or high-k dielectric, but it must reduce the gate leakage current of the device so as to improve the gate control capability of the device.
  - Using a channel alignment technique to form a non-polar surface channel to obtain a high mobility non-polar surface of SiC MOSFET device.
  - For the DMOSFET structure, the split-gate structure can be used to reduce the gate contact area of the JFET region, thereby effectively reducing the gate-drain capacitance, and the gate charge of the device is greatly reduced, so that the dynamic switching performance of the SiC MOSFET device is greatly improved.
  - For the UMOSFET structures, a bottom-thickened gate dielectric structure can be used to reduce Miller capacitance and Miller charge, thereby reducing the dynamic switching losses of SiC MOSFET devices.
  - It is common to implant a p-type shield on the bottom of the trench to protect the structure of the trench gate dielectric. The current leading technology is Rom's dual-trench structure, which implants a deep p-layer to protect the oxide at the bottom of the gate through the bottom of the source, and Infineon's single-channel shielded UMOSFET structure optimizes the gap of the p-type shield to obtain SiC UMOSFET devices with low on-resistance and high gate oxide reliability. We believe that the structures of SiC UMOSFET are various in the future. The gate structure will be adopted a more precise three-dimensional structure, and the oxide layer at the bottom of the gate trench will be protected so that the static conduction characteristics and the reverse blocking feature can be greatly improved. At the same time, as the channel resistance of the SiC UMOSFET decreases, the area of the SiC UMOSFET device of the same current will be greatly reduced, so that the effective gate capacitance is also proportionally decreased. Therefore, the dynamic performance of the device will be significantly enhanced. In the future, the overall market share of SiC MOSFET devices will maintain a steady increase of 30%, and the UMOSFET structure in MOSFET devices will gradually expand its market share.

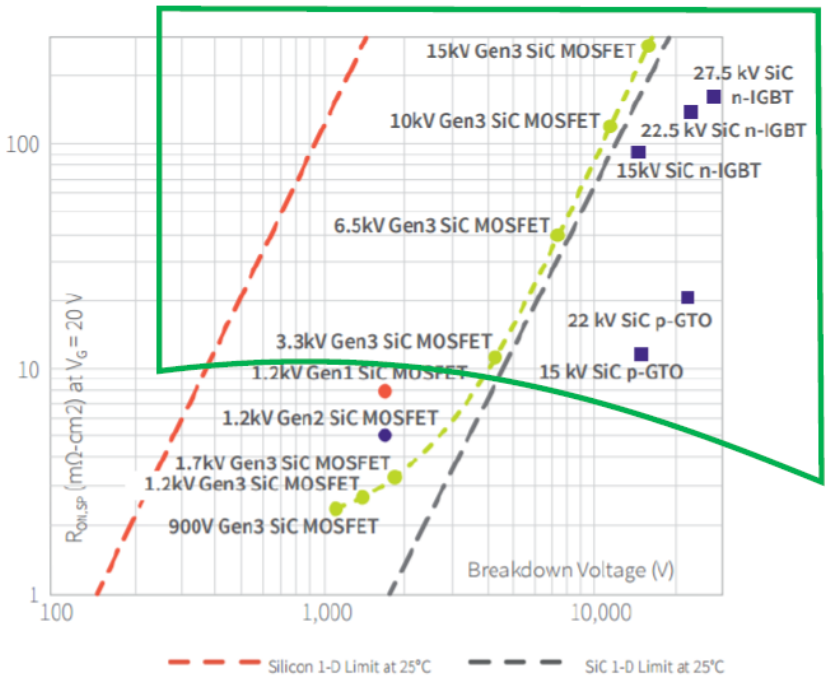


Fig 1.12 Current current voltage level of SiC MOSFET

Chart1.1 Forecast of power device development

	2020	2025	2030	2035	2040	2048
Schottky diode V/I	600V~1700V/~150A	600V~6500V/~200A	600V~10kV/~400A			
PiN diode	10kv~18kV/~10A	10kv~25kV/~50A	10kv~30kV/~100A	10kv~30kV/~200A	10kv~30kV/~300A	10kv~30kV/~400A
MOSFET V/Ω	600V~1700V/~150A	600V~6500V/~200A	600V~10kV/~400A			
GTO V/I		10kv~30kV/~50A	10kv~30kV/~150A	10kv~30kV/~300A	10kv~30kV/~500A	10kv~30kV/~1000A
IGBT V/I	10kv~18kV/~10A	10kv~25kV/~50A	10kv~30kV/~100A	10kv~30kV/~200A	10kv~30kV/~300A	10kv~30kV/~400A

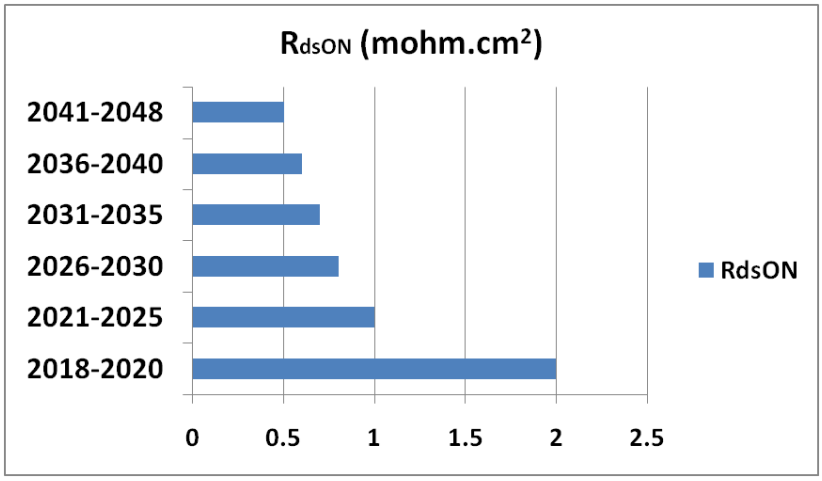


Fig 1.13 The specific on-resistance of SiC MOSFET

- Integrated device development of SiC MOSFET: (as shown in Fig 1.14[5])
  - Several applications of SiC MOSFET-based circuits, including switching power supplies, adjustable speed drivers, etc., the excess current flowing through the parasitic diodes within the MOSFET power device during the operating cycle. When used as a front-end switch for a power converter, the body diode of the power MOSFET acts as a flyback diode that flows through half of the current during the power conversion cycle. The stored charge of the SiC PN diode causes the MOSFET power device to generate additional reverse recovery current, so the parasitic SiC PN junction diode limits the device's safe operating area (SOA), turn-off loss, and switching speed.
  - Due to the increased electrical performance of SiC chips, there is an increasing demand for integrated manufacturing of devices. The so-called SiC MOSFET integrated device refers to the technology of integrating SiC MOSFET and SiC SBD into one cell for chip layout and optimization. The high-frequency operation of the device in the first quadrant is still controlled by the gate of the SiC MOSFET, while in the third quadrant, the flyback operation is mainly performed by the internal Schottky device. This saves the peripheral parallel diode to a certain extent, reduces the chip area integration overall. It can also accelerate the reverse recovery of the body diode, reduce the on-resistance of the device, improve the device's figure of merit, and overall reduce the SiC MOSFET device and Schottky device manufacturing costs.
  - Optimized structural design improves device performance by integrating Schottky devices, such as rationally arranging the SiC Schottky contact area and the MOSFET active area the current sharing design of the carrier conduction path in the drift region, and the shielding design of the leakage current during blocking. Enhance the functionality and efficiency of individual cells in a semiconductor device through miniaturization and integration of devices.

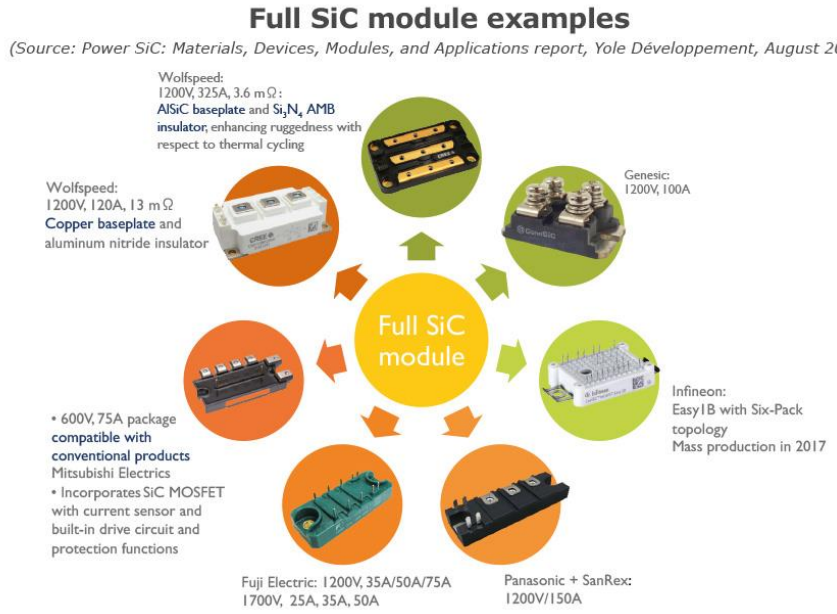


Fig 1.14 SiC module performance with integrated SiC MOSFET and SBD devices

1.3.2.3 Materials and processes

- **SiC Schottky device**

➢ Development trend of processes:

- The contact of Metal and SiC semiconductor is the most basic and core structure of SiC Schottky devices. It is the hub responsible for device energy input/output. Corresponding to ohmic contact is Schottky contact. SiC Schottky devices operate in the high-frequency, high-temperature environment, and the electrical performance of SiC diodes will be significantly affected. When used in extreme military or space environments, the Schottky barrier of the SiC device is reduced after irradiation, resulting in increased leakage current of the device during reverse bias operation. The control of Schottky contacts is an important process technology in the fabrication of SiC Schottky devices. To ensure uniformity of lateral Schottky barrier of the device, to improve the reproducibility of SiC Schottky devices

➢ Challenge:

- Firstly, how to form a well-connected Schottky contact with the rectifying effect. Secondly, how to adjust the interface state and the barrier height, so that the reverse leakage of the SiC Schottky device can be reduced. Thirdly, how to ensure the consistency of barrier height to increase wafer throughput.

➢ Potential solution:

- The forward current transport model of SiC Schottky diode is established

according to the regulation mechanism of different surface doping concentration on SiC Schottky rectification characteristics. Study on the electron transport mechanism of SiC surface under different process conditions.

- Develop new surface treatment technology to control the barrier height and surface state of metal/SiC contacts. At present, Ti is a common metal for SiC Schottky contact. As an alternative, the contact process of Al-based metal and SiC interface needs more development.
- Study the relationship between the barrier height of SiC Schottky devices and the temperature field and radiation field. Research the dependence of the ideal factor n on temperature. Improve the Schottky contact inhomogeneity theory, including the influence of surface doping concentration non-uniformity, the chemical reaction in the interface and the non-uniformity of the surface state of Schottky contact in different distribution ranges.

■ **SiC MOSFET device**

➢ Development trend of processes: (as shown in Fig 1.15)

- The fabrication process of SiC MOSFET is much more complicated than SiC Schottky devices, including n- and p-type ohmic contact process techniques based on ion implantation, getting n- and p-type ohmic contacts close to the epitaxial process. In the current mainstream SiC MOSFET devices, the n-type specific contact resistivity is ≤5×10-5Ω.cm^2, and the p-type specific contact resistivity is ≤10-5Ω.cm^2, but the performance degradation is obvious during high-temperature aging. Then we believe that in the future, in SiC ohmic contact process: n-type specific contact resistivity ≤ 5 × 10-7 Ω.cm^2, p-type specific contact resistivity ≤ 10-6 Ω.cm^{2,} and during 100 hours 600℃ aging test, ohms contact resistivity and the mechanical joint strength are not significantly degraded.
- High activation rate surface and smoothing ion implantation doping process technology. SiC is different from conventional Si-based devices, which can be doped by diffusion methods. The impurity diffusion coefficient in SiC is very small, the temperature at which the diffusion condition is reached is very high, and the high temperature causes the SiC material to be denatured. Usually, a high-temperature ion implantation process is used. Currently, the active region doping of the SiC MOSFET device including n-well and p-well, terminal, source area, base area, etc. need the ion implantation process.
- Gate oxygen oxidation and nitriding technology for SiC MOSFET. Thermal oxidation growth gate SiO_2 is the most mature technology on silicon. SiO_2 layer has the best compactness and pressure resistance. However, there are C atoms in SiC, the aggregation and vacancy of C atoms on the surface make the MOS interface have more interface states, which is about 2-3 orders of magnitude higher than silicon. This is also a technical difficulty of SiC MOS. Thermal oxidation above high

temperature (1300 °C) can effectively reduce deep level traps, while oxidation or thermal oxidation annealing in NO, N_2O atmospheres can effectively passivate interface dangling bonds, thereby improving interface states.

- Physical and chemical mechanism and morphology control technology for wide bandgap semiconductor etching. The trench type SiC MOSFET device requires an etching process to replicate the sidewall morphology of the mask at a certain ratio while ensuring a smooth surface and no over-etched micro-grooves at the bottom of the sidewall. Especially for high-voltage devices, these topographical parameters directly affect the withstand voltage performance of the device. Failure to do so at any point will result in partial premature breakdown. On the basis of ensuring the above key indicators, it is also necessary to optimize the etching uniformity in the wafer through process window optimization.

➢ Challenge:

- Controlling the SiC gate-oxide thermal growth process and annealing process technology, reducing the SiC MOS interface state and improving the channel mobility are major challenges in enhancing the performance of SiC MOSFET devices.
- Lattice damage caused by high-dose and high-energy ion implantation, activation efficiency at high temperature, and repair of lattice defects are key processes in the fabrication of SiC MOSFET devices.
- SiC trench etching technology and interface repair technology after etching are important means to improve trench SiC MOSFET devices.

➢ Potential solution:

- The N-atom passivation technology, P atom passivation technology, Sb atom passivation technology, and high-temperature oxidation annealing process are used to reduce the interface trap state. Improve channel mobility and increase gate dielectric reliability. The high-k material such as Al_2O_3, AlON is used as the SiC MOS gate dielectric, or the high-k/SiO_2 composite material is used as the SiC MOS gate dielectric. The new oxide annealing process for developing SiC non-polar surfaces is another way to enhance the forward conduction performance of SiC MOSFET. At present, the interface state density of the SiO_2/SiC interface of conventional SiC MOSFET is about 1012eV-1cm^{-2}, and the channel field mobility is 30-50cm^2/V.s. In the future, it is hoped that the interface state will be reduced to 5×1011eV-1cm^{-2} or less by the new SiC oxidation process, and the channel field mobility is increased to 100cm^2/Vs or more.
- Combined with the device preparation process, the effects of process parameters such as temperature, time, temperature increase and decrease rate and atmosphere on the activation of impurities and lattice recovery process should be systematically studied. The process of impurity activation and lattice recovery should be considered to analyze the roles played by these factors. The effects of ion implantation and annealing

activation processes on the blocking ability, on-state resistance and switching speed of SiC devices need to be investigated. At present, the conventional energy for ion implantation of SiC MOSFET devices is 700 keV. We believe that SiC implantation can advance toward the range of MeV energy, and the increase of injection energy can make us obtain a special structure of SiC MOSFET devices, such as super junction structures, which has greatly improved the overall performance of the device. At the same time, the target of high-temperature high-energy ion implantation of SiC is: surface roughness ≤ 5nm, injection activation rate is not less than 90%, and the uniformity of annealing activation carrier concentration is ≤ 10%.

- Gate trench etching requires the formation of a good sidewall with less roughness to reduce the reverse leakage characteristics of the SiC MOSFET device. The gate trench needs to form a better collimation, sub-trenching structure to improve the reverse breakdown reliability of the device. Etch mask selection ratio and precise control of SiC etch rate: adjusting etching power and chamber pressure control the morphology and rate of etched SiC by adjusting the ratio of etching gas, such as fluorine-based gas, oxygen, etc. SiC mild slope etching process: 4-inch SiC mild slope ≤ 30 °, no micro-grooves, etch depth uniformity deviation ≤ 5%, surface roughness ≤ 5nm.

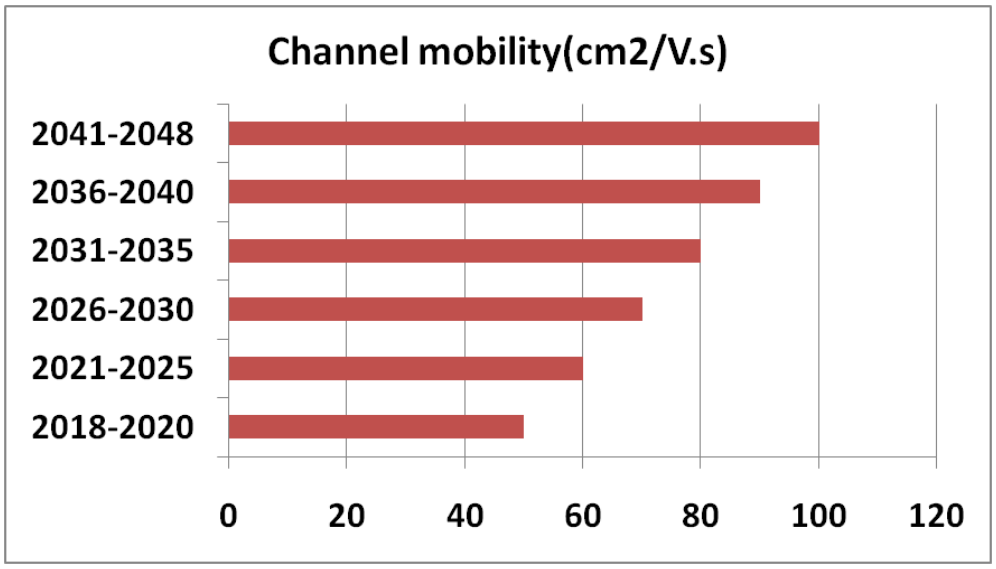


Fig 1.15 Channel mobility development of SiC

1.3.2.4 Packaging and heat dissipation

- **SiC Schottky device**

➢ Development trend of packaging

- SiC is a revolutionary semiconductor material used in power electronics. Compared to Si Schottky devices, its key features include superior

switching performance, no reverse current, and temperature that hardly affects switching behavior and wide operating temperature range -55 ° C - 175 ° C. However, as the on-resistance of SiC Schottky devices continues to decrease, the packaging requirements for SiC Schottky devices are becoming higher and higher. Due to the fact when Schottky diodes operate under high current conditions, it will have significant heating effects so that the reliability of the device will be affected. With the application of high-power SiC Schottky diodes, device packages related to lowering thermal resistance and maintaining good heat dissipation are receiving more and more attention.

- Challenge:
  - While improving the miniaturization of the device, how to reduce the thermal resistance of the internal chip to the pin, effectively improve the heat dissipation area inside the device, and make up for the heat dissipation defect of the internal isolation layer are important challenges for the packaging and heat dissipation of the SiC Schottky device.
- Potential solution:
  - Improve device package design, including packaging materials, structural improvements.
  - Selecting materials with excellent insulation properties and high thermal conductivity as the substrate material of the device package such as aluminum nitride, aluminum oxide, etc. which can transfer the power consumption heat source of the chip well. Materials with a thermal expansion coefficient close to SiC can effectively avoid thermal stress caused by temperature changes.
  - Select a more reliable patch material to bond the silicon carbide chip to the substrate. Common materials such as Ag/Ag nanoparticles/Ag glass, Ag-Au alloy materials, etc.
  - Select a bonding metal material with a melting point greater than 600 °C, such as Al, Au, Pt, etc. Generally, the bonding metal material should be consistent with the electrode metal material of the SiC Schottky device, so that internal diffusion of the metal will not happen and the structure is stable.

■ **SiC MOSFET device**

- Development trend of packaging: (as shown in Fig 1.16[6])
  - As the size of the chip shrinks, the power density of SiC MOSFET devices increases, which makes the requirements of parasitic inductance and capacitance of the package more stringent. Since the SiC MOSFET operates in the high-frequency environment, and the gate dielectric of the device is susceptible to electrical stress leading to degenerate. Therefore, the device package of the SiC MOSFET should be distinguished from the packaging technology of the conventional Si-based MOSFET.
  - The packaging material also brings lead resistance. Reduce SiC MOSFET

gate resistance, minimize switching energy consumption, to improve device maximum switching frequency, stability, and short-circuit tolerance.

- Thanks to the improvement of the heat dissipation capability of the package and the characteristics of SiC high-temperature operation and high-temperature packaging technology, the power density of SiC MOSFETs will continue to increase significantly in the future. The integrated package of SiC SBD device and SiC MOSFET device can greatly reduce the forward voltage drop of the internal diode, achieve lower loss, and reduce the number of components, thus achieving chip size miniaturization.

➢ Challenge:

- In addition to the same problems faced by SiC Schottky devices, SiC MOSFET device packages must also face the challenges of gate oxide films that are prone to failure.

➢ Potential solution:

- Improve the internal package gate contact resistance of the device, improve the consistency and high frequency of device switching control.
- Reduce parasitic inductance, improve power cycle capability and anti-interference of electrical oscillation of dI/dt, dV/dt. At present, the electrical oscillation of most SiC MOSFET causes the operating voltage of the gate dielectric to exceed the rated +20/-10 range, thus causing the device to fail.
- High-temperature packaging technology with high thermal conductivity and high thermal expansion matching. Packaging materials must have operating characteristics of high temperature and high electric field.
- Improved EMI capability and self-heat management performance.
- Use SiC MOSFET 4-lead package technology, which provides additional emitter terminals to reduce source stray inductance, to increase the switching frequency of the device, and reduce gate dielectric impact on SiC MOSFET devices.

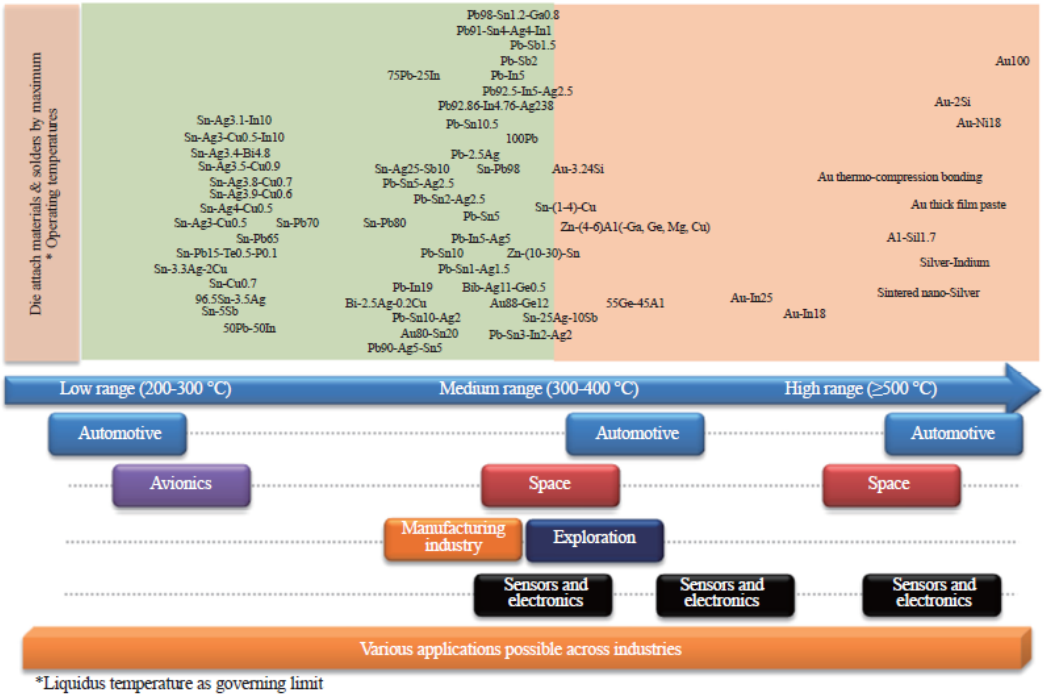


Fig 1.16 Materials that can be used in SiC power device packages in the future

1.3.2.5 Reliability

- **SiC Schottky device**

➢ Development trend of reliability:

- Due to its high thermal conductivity and large band gap, SiC materials have strong application potential under high-temperature conditions. However, due to various problems of SiC material quality and process, SiC Schottky devices still face various reliability problem.
- When the SiC Schottky device is in reverse bias, the electron emission from the metal to the semiconductor dominates. Ideally, the reverse current is a constant value, but in actual cases, the device has a large leakage current. With the increase in temperature and the number of switching, this leakage will lead to the increased power consumption of the circuit, and it will cause thermal out of control .
- The turn-off loss of the SiC JBS Schottky device is much higher at 300 °C than usual, while the turn-off loss of the SBD Schottky device does not change much with temperature. However, JBS Schottky devices have better surge voltage reliability, while SiC SBD devices experience repeated surge current surges, the device's ability to withstand surge voltages decreases, and the device's turn-on voltage drop rises.
- The package type has an important influence on the reliability of SiC Schottky devices. The forward voltage drop and reverse bias leakage of the SiC Schottky device in the TO220–Green A package after the

1000-hour high-temperature anti-aging experiment are stable. However, the forward voltage drop and reverse bias leakage of the SiC Schottky device in the TO220–STD package after the 100-hour high-temperature anti-aging experiment change a lot, and the device fails.

■ **SiC MOSFET device**

➢ Development trend of reliability:

- Although research on SiC MOSFET devices has been around for 20 years, the implementation of high-reliability MOS-based SiC power devices faces significant physical challenges due to the presence of tunneling currents in the oxide layer. This tunneling mechanism causes carriers to be emitted into the dielectric and induces time-dependent dielectric breakdown (TDDB) and Fowler–Nordheim tunneling.
- SiC MOSFET devices operate in high-energy particle environments, which can cause vacancies, gaps, and other related defects. The energy states induced by these defects affect the electrical properties of materials and devices. Exposure to 100k rad MOS capacitors (n-type epitaxial, oxide thickness is 67.5nm), the interface state density changes little, but produces a flat-band voltage shift of about -1.2 V, due to the combined effect of trapped charge of radiation-induced oxides and the trapped charge of the deep level interface (trapped by hole). After the irradiated, the interface state density of the device has a large increase.If the radiation dose is changed from 100 to 600 kilo cd, the calculated interface state densities are 6×1011 eV-1.cm^{-2} and 1.3×1012 eV-1.cm^{-2}, respectively.
- At 375 °C, the SiC MOS capacitor formed by thermal oxygen still has intrinsic reliability. When the electric field is less than 3.9 MV/cm, the working life can reach 100 years. The results show that the barrier height of 4H-SiC/SiO_2 is 2.57 eV (room temperature) and 2.36 eV (200 °C), which does not change sharply with temperature. For SiC MOSFET devices, the high-temperature stress reliability is greatly reduced compared with the MOS capacitor because the subsequent process has undergone ion implantation annealing and a terminal oxide layer on the periphery of the device. At 175 °C, 3 MV/cm, the dielectric breakdown test of 2 KV DMOSFET can have an average life of up to 100 years, about two orders of magnitude lower than MOS capacitors. Reliability under high thermal stress also is exhibited by the stability of the MOSFET threshold voltage and the magnitude of the reverse leakage current. Positive bias causes a positive shift of threshold voltage, negative bias moves negatively, and increases with offset amplitude.
- The thermal stress failure mechanism of SiC MOSFET devices is different from that of Si-based. The latter is mostly due to the physical reasons of the device materials. The former is mostly caused by structural design defects such as termination structures. If the design can be optimized on the structure and package, the material properties of the SiC wide band

gap can be fully utilized and the thermal stress reliability can be improved. The superiority of SiC MOSFET devices over Si MOSFET devices is also reflected in higher frequencies and higher load currents. The same problem faced by the former is that the repeated load power consumption changes cause the periodic change of the junction temperature of the device, which causes thermal stress damage to the inside of the package of the SiC-based MOSFET. The lifetime of high-voltage SiC power MOSFET is also subject to degradation of some electrical and mechanical interconnects, such as solder joints, bond wires, and the link between tube and core. This degradation mechanism is by a mismatch in the thermal expansion coefficient at the interface or a thermoelectric stress generated by temperature fluctuations during high-frequency operation.

1.3.3 Si-based GaN epitaxy and power devices

1.3.3.1 Si-based GaN epitaxy

- Development trend: (as shown in Fig1.17)
  - The marketization process of Si-based GaN power electronic devices requires the cost of material epitaxy to decrease.
  - The size of the Si substrate used for GaN epitaxy in the next 30 years will be extended from 6 inches to 8 inches in the next 5 years and will expand to 12 inches or even 18 inches in the next 10-15 years.
  - In the case of gradually grasping the mechanism of epitaxial leakage and the influence mechanism on the dynamic performance of the device, the epitaxial quality is continuously improved on the basis of reducing the epitaxial thickness. For example, the epitaxial thickness suitable for 650 V products is thinned from the currently used ~5 μm to ~ 3 μm.
- Challenge:
  - Stress control and yield for large-scale epitaxy.
  - Uniformity of large-scale epitaxy.
  - The long-term effects of epitaxial parameters on device dynamic performance and reliability are still unclear.
  - Potential solution:
  - Stress control relies on in-situ detection and stress compensation during epitaxial growth.
  - Uniformity depends on the upgrading of epitaxial equipment and accurate modeling of growth dynamics.
  - The effect of epitaxial parameters on device performance and reliability depends on the accumulation of data.

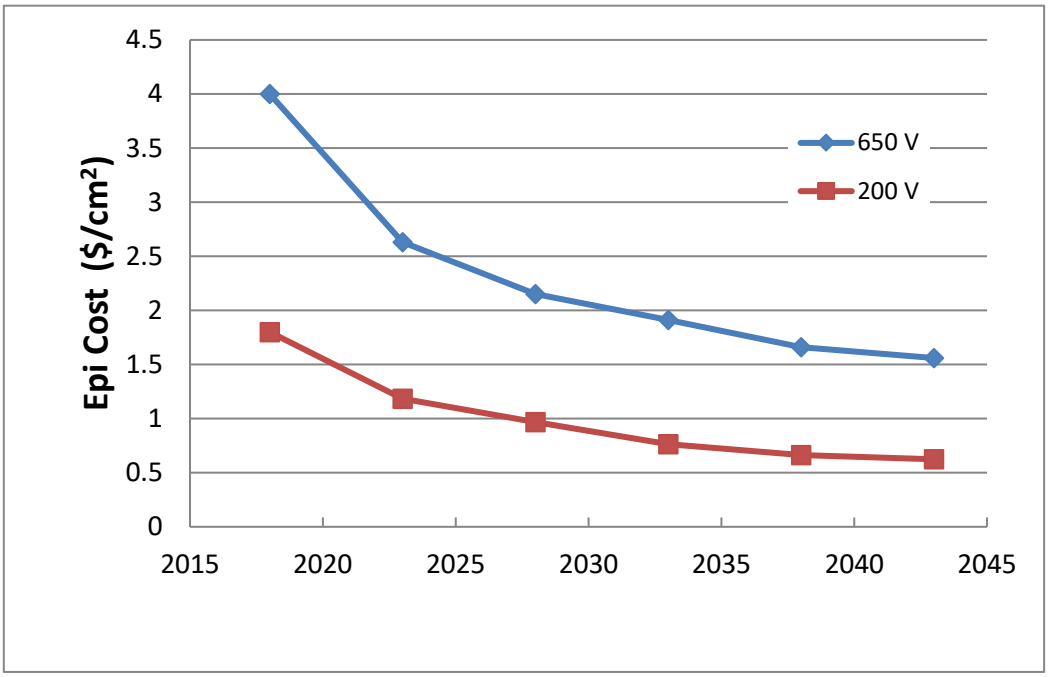


Fig 1.17 Development trend of 650 V/200 V Si-based GaN epitaxy

1.3.3.2 Si-based GaN power device

- **Withstanding voltage level of the device**
  - Development trend: (as shown in Fig1.18)
    - The withstanding voltage level of Si-based GaN power electronic devices is expected to increase from the current 600/650 V to 1200 V in the next 5-10 years, and then will be in a stable state, mainly due to both technical and market factors; vertical GaN power electronics are more subject to cost, so no market forecast is made here.
    - 600/650 V products have the largest market share, and it is predicted that 600/650 V products will account for 80% of the GaN market share after market formation, while 900/1200 V devices and 200 V devices account for 10% each.
  - Challenge:
    - Technical: There are more uncertainties in the dynamic performance and reliability of GaN power electronic devices under higher electric fields.
    - Market: With the continuous optimization of GaN power electronic device development and production control, the cost is gradually reduced; but due to the cost reduction of large-size SiC substrate, the mainstream application of GaN power electronic devices is 1200 V and below.
  - Potential solution:
    - In the 900 V and 1200 V areas, it is necessary to increase the epitaxial thickness to increase the withstanding voltage in the vertical direction, while optimizing the field plate structure and regulating the electric field

distribution.

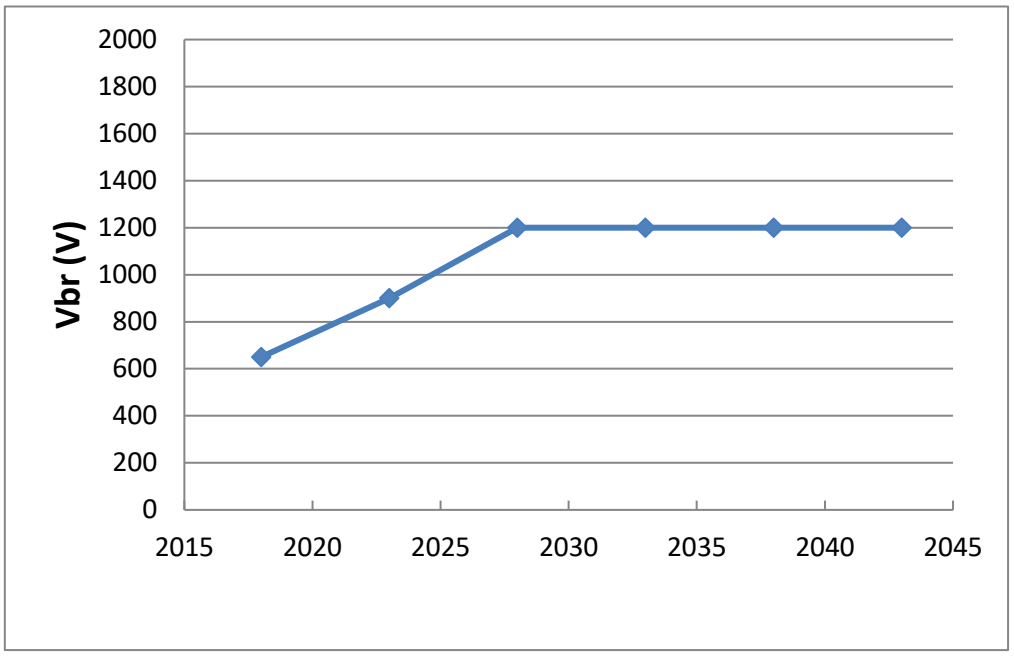


Fig 1.18 Development trend of withstand voltage level of Si-based GaN power electronic devices

■ **Structure of device**

➢ Development trend: (as shown in Fig1.19)

- At present, there are only a handful of IDM companies in the industry to promote cascading devices. Many companies (especially design companies) promote enhanced devices based on the foundry model. In terms of product performance, the cascode cascading device in practical applications above 600 V is easy to achieve marketization in the short term, and its market share will occupy 50% in 10 years. With the mature of E-mode device technology, the share of cascode will be reduced and at last, it will only have part of the share of 1200V.
- Based on the need to further reduce costs and improve performance, E-mode devices will occupy the majority of the market share after the technology matures, but the time required will be quite long.

➢ Challenge:

- Cascaded devices face the problem of packaging cost and the problem that the single-tube current of multi-chip micro-modules cannot be further increased.
- Enhanced devices are more subject to fundamental and functional issues, such as threshold voltage, gate withstanding voltage is not high enough, threshold voltage drift, hard drives in applications, etc.

➢ Potential solution:

- Cascaded devices increase output current and output power in parallel.
- Enhanced devices require the introduction of a more withstand voltage gate dielectric layer and a smaller interface charge to get higher threshold voltage and gate withstanding voltage.

- Develop dedicated drivers for enhanced devices or different drive methods such as current drive.

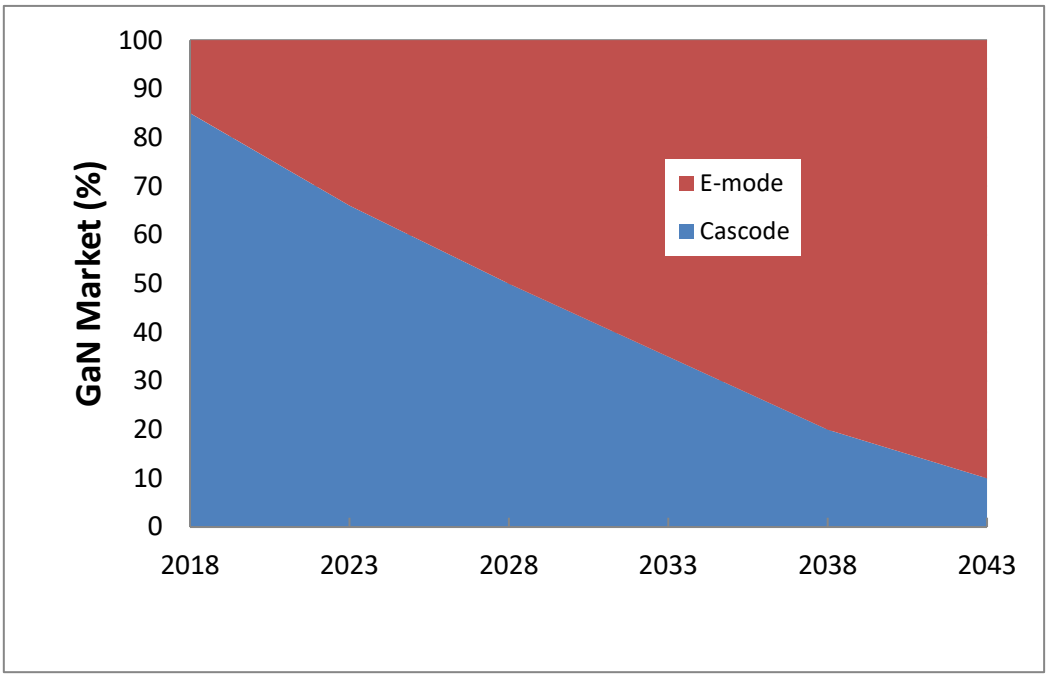


Fig 1.19 Development trend of market share of different device structures in the GaN power electronics

■ **The current density of the device**

➢ Development trend: (as shown in Fig1.20)

- Based on the requirements of both device performance and control cost, the current density of the device is continuously increased, that is, the Ron*Qg or the characteristic resistance Ron*Area of the device is continuously reduced. In the next 30 years, the current density of 650 V devices will be doubled from the current 1.8 A/mm^2, and the current density of 100 V devices will now increase from 4.1 A/mm^2 to 6.5 A/mm^2.

➢ Challenge:

- The increase in current density makes high demands on the heat dissipation of the device.
- The size of the device's field plate and the reduction of the spacing between the electrodes pose a high challenge to device reliability.

➢ Potential solution:

- Device cooling depends on new packaging technologies and substrates with higher thermal conductivity, heat sinks, etc.
- Increased investment in the study of reliability to establish failure models and device life-dependent size models.

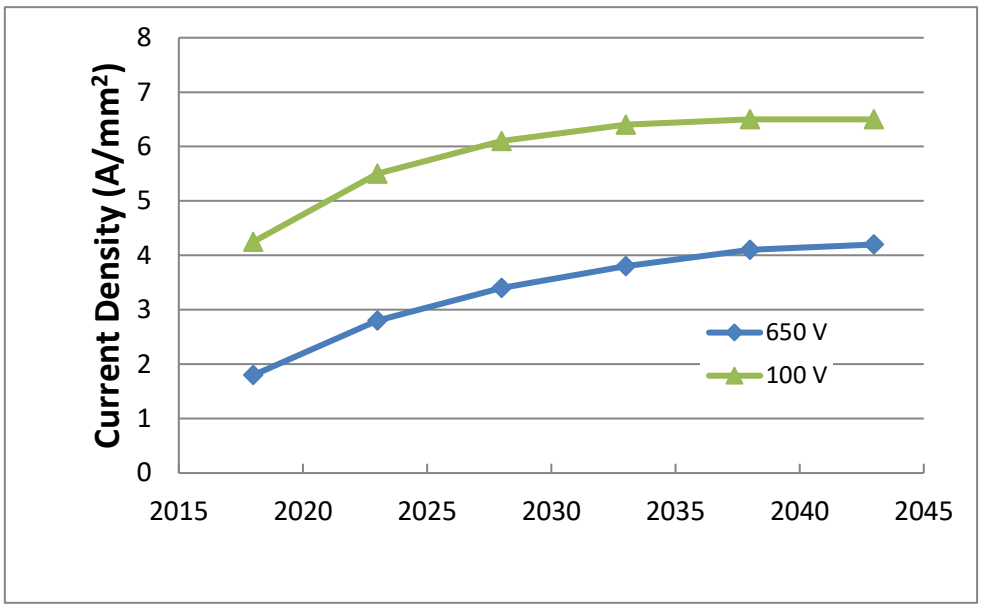


Fig 1.20 Current trends in GaN power electronics current density

■ **Chip package form**

➢ Development trend: (as shown in Fig1.21)

- The main form of power electronics package is TO series (including TO-220/247, etc., major manufacturers are Transphorm, Panasonic, etc.), SMD series (including QFN/DFN, etc., major manufacturers are Transphorm, Panasonic, etc.) and module package. In addition to the above-mentioned conventional forms, the package form of GaN chips currently available on the market includes low-voltage devices LGA packages (EPC), Power IC packages with integrated drivers and other components (TI, Navitas, etc.) and others (such as GaN Systems embedded).
- TO package as the traditional mainstream packaging form of power electronic devices is also the main packaging form of GaN devices. In the current, GaN power electronic device market is not fully opened, all kinds of new packages are emerging. The market share of TO package will be from the current 30% to 45% with the update of mainstream power electronics applications.
- The inductance of the traditional SMD surface mount package is slightly smaller than that of the TO package, but the heat dissipation capability is slightly worse. About 20% of the current market share will shift with the high-frequency application technology to the power integration type, that is, the Power IC package form.
- Integrated driver-type Power ICs can take full advantage of the high-frequency characteristic of GaN devices. As the technology of high-frequency applications continues to mature, its market share will rise to 10% in the next 30 years.
- The market share of low-voltage products below 200 V will be squeezed

to below 10% as the mainstream 600/650 V market matures.

- The market share of module applications will exceed 12% with the increase in application requirements above 5 kW and the maturity of the technology.
- Other packaging forms will maintain a market share of around 10%. Some existing products are difficult to break through the limitations of thermal performance. There is limited room for development, but I believe there will be more complete package forms.

➢ Challenge:

- As the current density or power density of the device increases, the heat dissipation of the chip will hinder the improvement of system integration.
- In high-frequency applications, the conversion efficiency is relatively low, and the power dissipation capability of the Power IC will cause negative feedback on the conversion efficiency.

➢ Potential solution:

- Device cooling depends on new packaging technologies and substrates with higher thermal conductivity, heat sinks, etc.
- For high-frequency applications above 5 MHz, develop dedicated drivers and low-loss cores for GaN devices, and optimized layout designs to improve system efficiency.

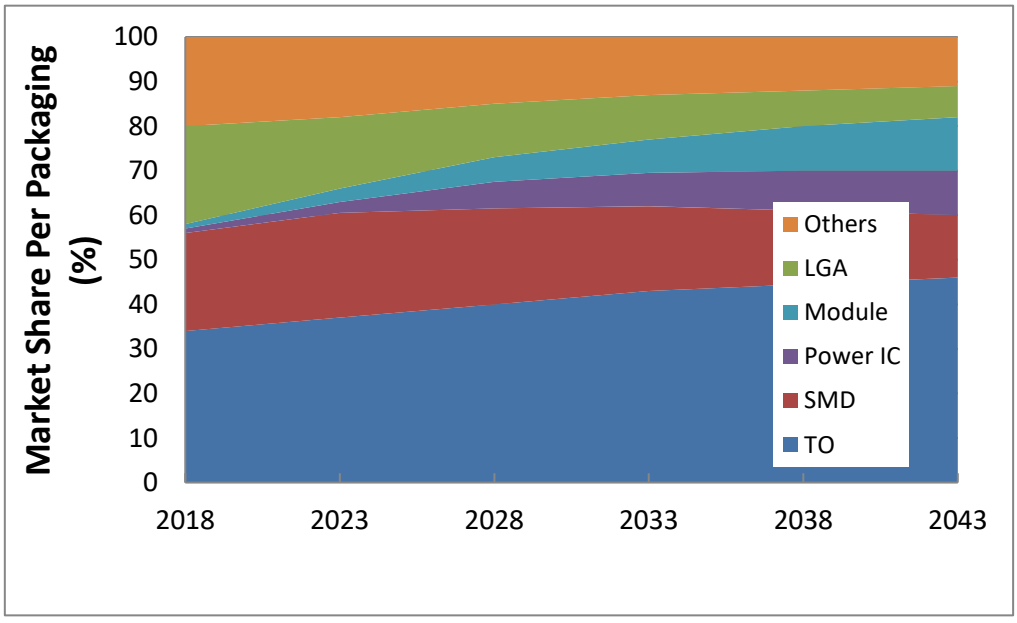


Fig 1.21 Development trend of chip packaging form

■ **Reliability**

➢ Development trend:

- The chip downstream industry has strict requirements on device reliability. This is another important factor that restricts the market development of GaN devices in addition to cost performance.
- GaN device vendors have tested reliability at different levels, and the published data shows that the device can work reliably for a long time.

- At the beginning, a series of tests were conducted on the long-term withstanding voltage and environmental resistance of the device using the JEDEC standard commonly used in Si devices, including high-temperature reverse bias, high acceleration temperature, and humidity, temperature cycling, power cycling, and life expectancy of high-temperature storage, etc.. High-temperature reverse bias is the key test for evaluating the withstand voltage of the device (temperature = 150℃, drain voltage = 80% of the voltage class, time 1000 hours). In 2012-2013, Transphorm announced that its 600 V GaN product is the first company in the world to pass the JEDEC standard test; so far, TSMC is another company that has announced that its product line is certified by this standard.
- For automotive electronics, Transphorm announced in 2016 that its products have passed the AEC-Q101 standard test, which has more test content and more stringent requirements on withstanding voltage of the device. For example, the drain voltage applied in the high-temperature reverse bias test is classified voltage. This standard lays the foundation for GaN devices to enter the automotive electronics market.
- In addition to the existing JEDEC and AEC-Q101 standards mentioned above, GaN device suppliers have released more application data for industry concerns about new products, such as Transphorm's release the 3000-hour HTOL data of GaN devices with 200V to 400V boost circuits at 175℃ junction temperature, which indicates that the conversion efficiency in the booster circuit remains unchanged during the 3000 hours of high-temperature application test, manifest that the performance parameters of the surface GaN device are less changed in the test.
- Further, by performing accelerated aging tests on GaN devices at higher voltages or higher junction temperatures, the average lifetime of the products at 650V and 150℃ junction temperatures is greater than 106 hours and114 years.

➢ <u>Challenge:</u>

- Integrating existing reliability data at different levels, downstream application vendors still have some doubts.
- The current reliability data is still based on the overengineering of extension, device, package, and test. The existing failure model may deviate from the actual situation on further improvement in performance and further cost reduction.

➢ <u>Potential solution:</u>

- In response to vendors' concerns about reliability, GaN device manufacturers need to work closely with downstream vendors to conduct small-scale trials in a certain application field and even provide non-recurring engineering (NRE) funds to promote marketization.
- Establish a failure model under various acceleration conditions and verify.

1.3.4 GaN single crystal substrate and vertical power device

1.3.4.1 GaN single crystal substrate and homoepitaxial

- **The diameter of the substrate**

➢ Development trend: (as shown in Fig 1.22)

- The diameter of the self-supporting GaN substrate currently used is mainly 50 mm. With the popularization and application of GaN-based optoelectronic devices and power electronic devices, and the cost control of device manufacturers, the development of large-diameter substrate materials has become an irresistible trend. The large-diameter substrate can effectively reduce the device fabrication cost, increase the available area of the chip per cycle, utilize the reaction chamber area more effectively, and significantly reduce the edge effects in subsequent processes.
- Therefore, it is expected that in the next 30 years, the proportion of large-diameter substrate will continue to increase; HVPE equipment and epitaxial technology development of 6-inch GaN substrate will be completed by 2020, and mass production of 6-inch substrate will be completed by 2025. Complete HVPE equipment and epitaxial technology development of 8-10 inchGaN substrate by 2030.
- At present, the mainstream manufacturers have completed the research and development of 100mm diameter GaN substrates, and are entering the mass production stage. Therefore, from 2019, the proportion of 50mm diameter GaN substrates will start to decrease year by year.
- A small number of manufacturers are working on 150mm diameter research and development, and they are close to completion by now, able to provide a small number of samples. It is estimated that in 2025, 150mm diameter substrates will enter the market.

➢ Challenge:

- Temperature field design and implementation: The suitable temperature field is the basis for the preparation of GaN single crystal. Unsuitable temperature field is very likely to cause cracking of single crystal and proliferation of crystal defects. The increase in the diameter of the single crystal causes a rapid increase in the size of the hot zone, resulting in a drastic increase in the design and implementation of the appropriate temperature field.
- Flow field and concentration field design and implementation: Unlike SiC, HVPE growth of GaN has stringent requirement on flow field and concentration field, and the expansion of reaction chamber and substrate size results in nonuniform distribution of input source gas concentration to form turbulence, pre-reaction enhancement, etc., which will affect

nucleation, uniformity and material quality. How to control flow and concentration fields to reduce turbulence and parasitic reactions is a key issue to consider for diameter expansion.

- Implementation of large-size single crystal lift-off technology: Since the only feasible solution for large-sized GaN single crystals is to use HVPE heteroepitaxial GaN thick films, the hetero-substrate is removed by laser lift-off or self-separation techniques. As the diameter size increases, the stability and reliability drop sharply, and the critical self-separation thickness increases sharply to the centimeter level, so it is currently difficult to achieve large-scale self-separation.
- Control of large-size single crystal stress and defect density: When using HVPE to grow large-sized GaN single crystal, due to large lattice mismatch and thermal mismatch stress and thickness non-uniformity, it is more likely to cause single crystal cracking and an increase of defect density. New epitaxial process technology should be developed to solve the problem of heteroepitaxial mismatch stress while reducing defect density and reducing process complexity.
- Large-scale preparation of GaN single crystal and cost: The production and cost of GaN single crystal is the bottleneck of large-scale application of optoelectronic devices, electronic devices, and microwave devices. How to improve the large-scale preparation level of GaN single crystal substrate and the cost reduction to acceptable levels for downstream companies for large-scale applications is the most critical issue for the GaN single crystal industry.

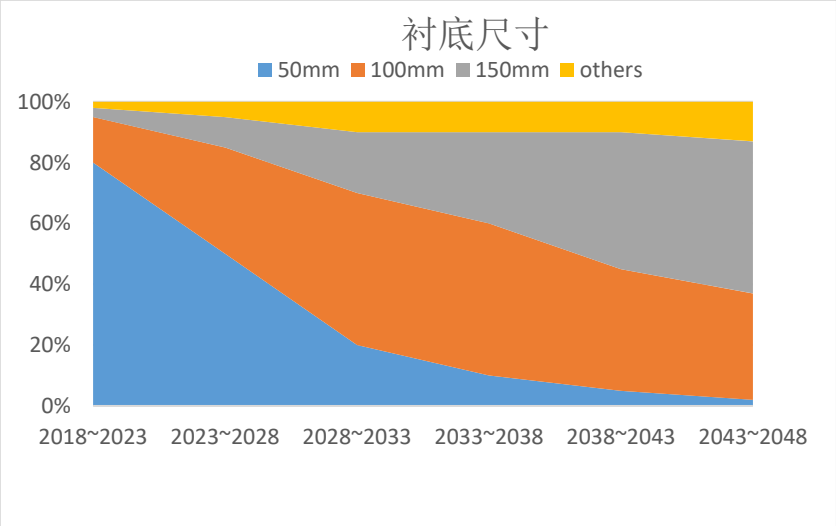


Fig 1.22 Development trend of GaN substrate

➢ Potential solution:

- Using numerical simulation to guide the design of large-scale single crystal growth thermal field, to achieve temperature field control in different growth stages.
- Study and analyze the intrinsic correlation and law of various key process

parameters, flow field turbulence and pre-reaction formation and evolution, establish non-equilibrium thermodynamics and dynamics model, simulate and optimize the physical field in the large-scale reaction chamber, and use numerical simulation to guide the design of large-scale GaN single crystal HVPE growth. The design of the flow field structure of the reaction chamber which can effectively weaken the flow field turbulence and pre-reaction is the key scientific problem and core technology for solving HVPE epitaxial growth of high-quality GaN materials.

- Develop new ideas for epitaxial processes and technologies to eliminate HVPE heteroepitaxial stress and reduce dislocation density.

■ **Crystalline defect density**

➢ Development trend: (as shown in Fig 1.23)

- With the rapid application of GaN-based optoelectronic devices and power electronic devices, the requirements for device performance and reliability are getting higher and higher. Crystal defects (such as V-pits, TSD, TED) in the substrate can have a negative impact on the device. At the same time, in recent years, the diversified single crystal defect elimination and conversion technology has developed rapidly, so it is expected that the density of crystal defects in the substrate will decrease.
- At present, mainstream manufacturers have the ability to prepare low V-pits density substrates ($<1/cm^2$), and the reduction of the density of threading screw dislocations (TSD) and threading edge dislocations (TED) will become the focus of research and development work of GaN substrate manufacturers. Therefore, it is expected that the density of TSD and TED in the substrate will continue to drop.

➢ Challenge:

- Cost: In order to reduce the density of crystal defects, the traditional process conditions cannot meet the growth of single crystals with low crystal defect density. It is necessary to introduce new processes and increase the complexity of the process, which will push up the cost of the single crystal.
- Size: With the increase of size, the residual stress in the single crystal increases, the size nonlinear effect is obvious and becomes the main influencing factor, the crystal quality is degraded, and the classical dislocation lateral bending and combining mechanism begin to fail. Compared to the 2-inch substrate, the trend of large-sized crystal defects density decreases tends to slow down. This contradiction will become the key to the future development of GaN single crystal substrates.

➢ Potential solution:

- Adopt new chamber design, minimize pre-reaction and ensure uniformity, reduce V-pits.
- Reduce the upper dislocation density by using a variety of twist dislocations combined with thickness extension techniques.

- Development of new single crystal growth techniques, such as ammonothermal methods and sodium flow methods, can essentially reduce the defect density of single crystals and eliminate V-pits.

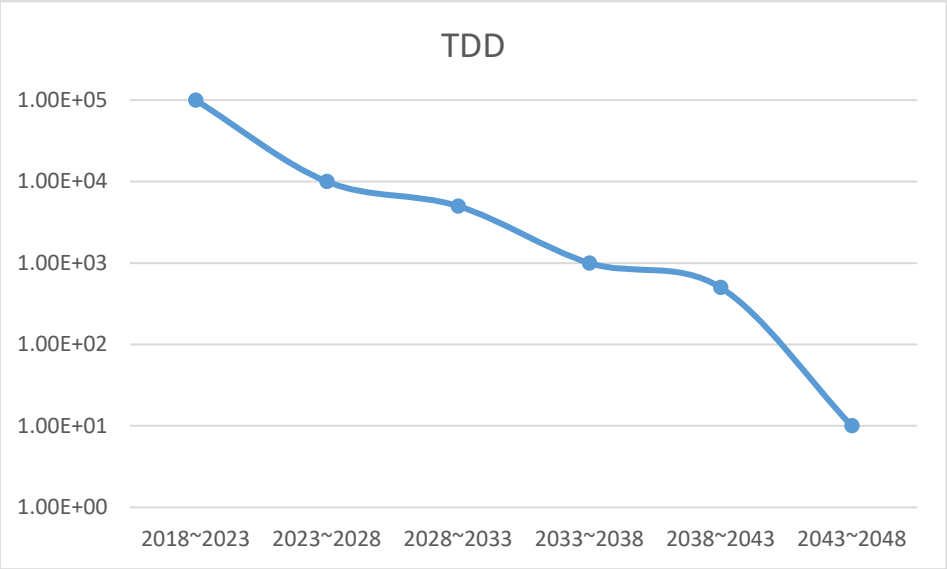


Fig 1.23 Development trend of the TDD of GaN substrate

■ **Unit area price of substrate**

➢ Development trend: (as shown in Fig 1.24)

- As the proportion of large-diameter substrates continues to increase, the cost the growth of per unit area of the substrate decreases. Taking a single crystal of 100 mm diameter and a single crystal of 50 mm diameter as an example, the cost ratio is about 1.0-1.5 times, and the available area ratio of a single substrate is 2.25:1.
- As the crystal defect density of the substrate decreases, the process complexity increases and the yield decreases in a short period, which will push up the price of the substrate.
- Neoteric single crystal growth technology, such as ammonothermal method, will rapidly reduce the price per unit area of GaN single crystal substrates.
- Based on the above points, in the recent 5 years, the unit area price of the substrate will be reduced slightly with the wide promotion of the diameter of 100mm substrate. After most substrate suppliers complete the low defect density single crystal growth process and surface treatment, the unit area price of the substrate will usher in a relatively rapid reduction.

➢ Challenge:

- Large-scale GaN equipment's development cost is high and the period is long: Since the large-sized GaN single crystal substrate still relies on the HVPE heteroepitaxial method, the corrosive environment makes the design of the large-sized reaction chamber difficult and costly. Heteroepitaxy makes it difficult to control the bending defect stress. Therefore, it is necessary to invest a large amount of time and material cost to develop new equipment and processes. A long development cycle

may hinder the cost reduction of per unit area of the substrate. For the ammonothermal method, due to the need to be used in high temperature and high-pressure growth environments, large diameter ammonia hot autoclaves are difficult to design and manufacture, and the verification cycle is long.

- As the size of the single crystal growth increases, the residual internal stress of the single crystal increases rapidly, causing bending cracking and difficulty in laser lift-off. How to take into account the single crystal size and single crystal quality are difficult.

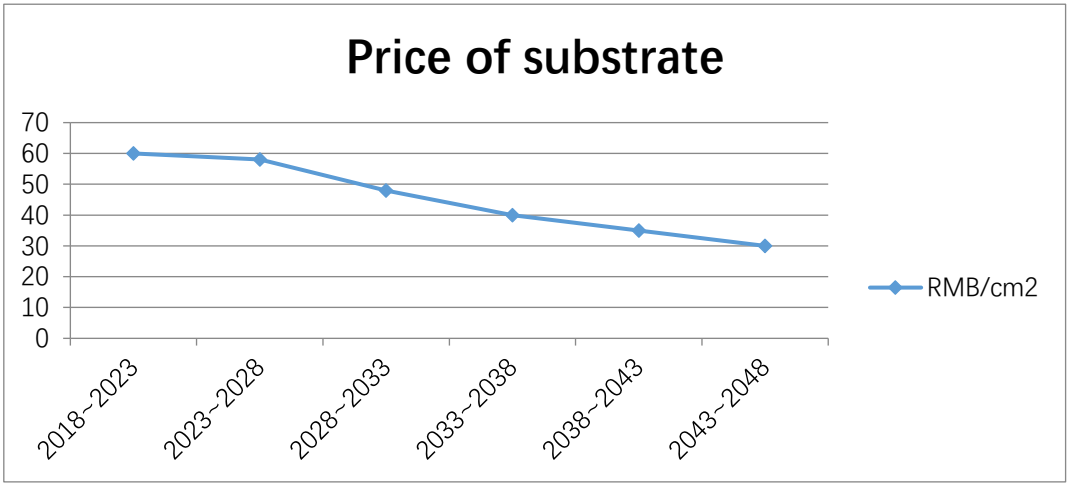


Fig 1.24 Development trend of the price of GaN substrate（RMB/cm^2）

■ **GaN homoepitaxy**

➢ Development trend:

- The current mainstream technology is the growth of homoepitaxial layers by metal organic chemical vapor deposition (MOCVD) on GaN single crystal substrates.
- The size of GaN-on-GaN homoepitaxial sheets depends mainly on the substrate size. At present, 50mm diameter homoepitaxial wafers have been mass-produced, and 100mm diameter homoepitaxial wafers have been customized for small batches. It is estimated that 150mm diameter homoepitaxial wafers will enter the market in 2025~2030, and in 2030~2048, the manufacturer will complete the development and mass production of 200mm diameter homoepitaxial wafer.
- At present, the maximum thickness of the n-type homoepitaxial layer is not less than 40μm, and the doping concentration is ~1016cm^{-3}. It is expected that the maximum thickness of the n-type epitaxial layer can reach not less than 80μm in 2030, and the doping concentration in 1015 cm^{-3}~10^{16}cm^{-3} range will be precise regulation.

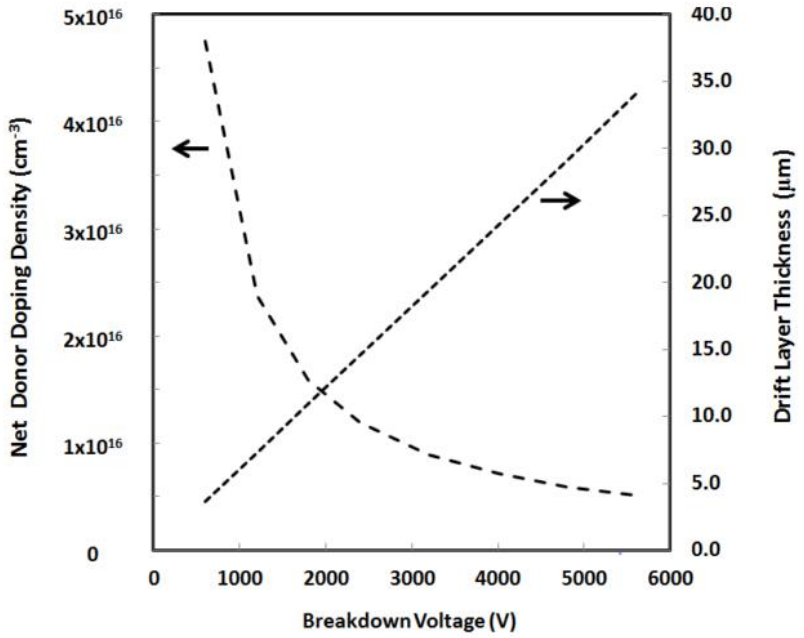


Fig 1.25 The relationship between epitaxial thickness, the doping concentration in the drift region and the breakdown voltage of GaN

- Challenge:
  - Doping concentration control of n-type GaN drift region: The doping concentration of drift region in the range of 1015cm^{-3}~1016cm^{-3} need to accurately adjust in kV-level vertical type device, while TMG gas used in MOCVD growth introduces C element and airtight problem introduces O element, which is not conducive to the precise regulation of the doping concentration of the n-type GaN drift region in the high voltage vertical device.
  - Integrated control of epitaxial size and epitaxial quality: As the size of single crystal substrate increases, it will become more difficult to reduce the background impurity concentration in the epitaxial process and control the homogenization material thickness, doping concentration, and carrier mobility uniformity.
- Potential solution:
  - Accurate regulation of doping concentration in n-type homoepitaxial materials by controlling key parameters such as pressure, temperature, and III/V ratio during MOCVD growth.

1.3.4.2 Vertical GaN power device

- **Vertical GaN Schottky Diode**
- Development trend:
  - Schottky devices have a wide range of applications in PFCs and power supplies. With the development and mature technology of single crystal

GaN substrates and homoepitaxial materials, the performance of vertical GaN Schottky diodes in forward conduction and reverse withstanding voltage is increasing; it is expected that within 10 years, relevant performance indicators will be further upgraded, and then enter the stationary period (as shown in Figure 1.26 [8]).

- Vertical GaN Schottky diodes are currently capable of withstanding voltage from 600V to 1000V. With the optimization of homoepitaxial thickness, doping concentration, and the junction termination protection technology for GaN devices, it is expected to reach 1500V~1700V in 2025~2030.
- At present, the specific on-resistance of 600V~1000V vertical Schottky devices has been reduced to ~1mΩ·cm^2, the forward turn-on voltage is 0.7V~1.0V, and the on-current is not lower than kA/cm^2. The specific on-resistance can be further reduced by increasing the electron mobility in the homoepitaxial material, thinning the substrate, etc., and the forward turn-on voltage can be further reduced by the Schottky metal work function control, thermal annealing, etc., to enhance Schottky interface features and reliability.
- Vertical GaN Schottky diodes have excellent switching and dynamic performance. The reverse recovery time t_{rr} is no higher than 20ns. The reverse recovery charge and on-resistance product (R_{ON}·Qrr) is not higher than 2Ω·nC, which is much better than Si-fast-recovery diode, slightly better than SiC Schottky diode.
- Vertical GaN Schottky diodes have been experimentally verified that there is no ubiquitous dynamic resistance degradation problem in planar GaN devices, which has advantages in high-efficiency high-voltage power electronics field.

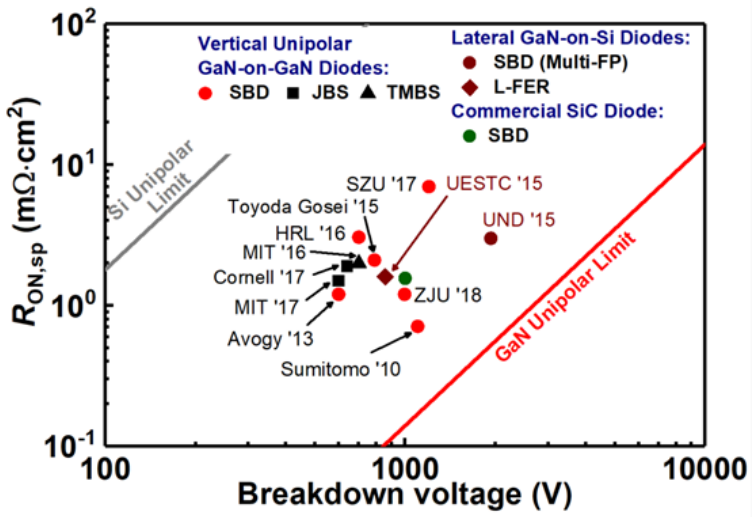


Fig 1.26 Development of GaNSchottky diode

➢ Challenge:

- Vertical GaN Schottky device termination protection technology: Due to the limitations of part P-type doping, terminal technologies such as JTE

and FLR widely used in Si and SiC devices are difficult to implement in vertical GaN devices. Therefore, there is an urgent need to develop effective terminal protection technologies and processes suitable for GaN devices to reduce reverse leakage current and increase withstanding voltage.

- High-quality Schottky contact: Schottky contact and interface quality directly affect performance characteristics such as turn-on voltage and reverse leakage current, which need to be improved from the metal work function, metal-semiconductors contact process, and homoepitaxial layer quality. The barrier reduction effect in the high field also causes an increase in the reverse leakage of the Schottky device.
- Long-term reliability: Although the dynamic and static performance of vertical GaN Schottky diodes has been initially verified, homogenous epitaxy can achieve higher material quality compared to heteroepitaxial, but for vertical GaN Schottky diode, the research of surge capacity, avalanche capacity and device lifetime are still in their infancy and require further experimental verification.
- Cost: GaN substrate costs are still large, reducing device materials and manufacturing costs remains an important challenge.

➢ Potential solution:

- Using plasma processing, ion implantation, trench and field plate combination method, develop high-efficiency terminal protection technology for GaN devices, suppress electric field concentration in the edge of the Schottky device junction and increase the withstanding voltage.
- Optimize the Schottky barrier height and the Schottky interface quality, reduce the turn-on voltage, and suppress reverse leakage for the turn-on voltage. Using a TMBS diode structure, the MIS structure of the bottom and sidewalls of the trench is used to shield the surface electric field of the Schottky contact; or the JBS diode structure is used to reduce the electric field of the Schottky contact surface by depletion of the lateral p-n region.
- Through the selective epitaxy of P-GaN or Mg ion implantation, research on devices such as GaN JBS/MPS can be carried out to improve the surge capability of the device. By optimizing the Schottky contact interface and improving the quality of the homoepitaxial material, the long-term reliability of the device can be enhanced.
- The development of large-size GaN single crystal substrates and substrate engineering technology helps to further reduce the cost of vertical GaN devices.

■ **Vertical GaN p-n diode**

➢ Development trend:

- The GaN p-n diode has low reverse leakage current and can reach higher voltage levels. Currently, 5.0kV vertical GaN p-n diodes have been realized, and Baliga's Figure of Merit (BFOM) can be up to 20GW/cm2

(as shown in Figure 1.27). With the development of GaN substrates, epitaxial material growth technology, and device process technology, it is expected that 10kV GaN p-n diodes can be realized in 10 years.

- Thanks to high-quality homoepitaxial materials, it has been observed that GaN p-n diodes have avalanche withstanding capability and can withstand higher avalanche electric strength at the same leakage current, achieving higher breakdown voltages.
- The minority carrier of GaN has a short lifetime, a short reverse recovery time, and a low reverse recovery charge. The reverse recovery time of the vertical GaN p-n diodes reported so far is no more than 50 ns, and the dynamic characteristics at 150 °C are basically unchanged. It is much better than the Si fast recovery diodes (100~500 ns), and slightly better than those of the SiC p-n diodes (~100ns).

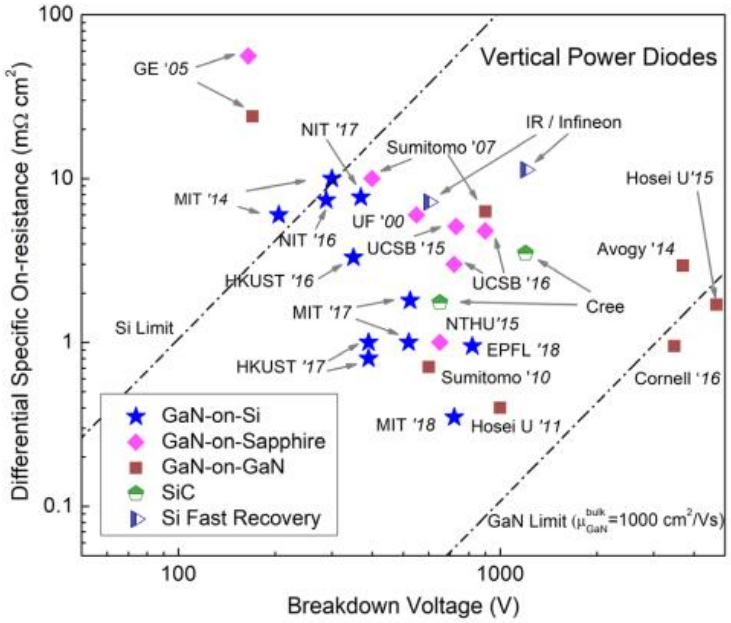


Fig 1.27 Comparison of GaN p-n diodes with other diodes.

➢ Challenge:

- Forward voltage drop: The wide band gap characteristic of GaN material causes the forward voltage drop of the p-n diode to be above 3V, resulting in large conduction loss. Large p-GaN ohmic resistance, also leading to an increase of forward voltage drop and conduction loss.
- Vertical GaN p-n device termination protection technology: Due to the limitations of part p-type doping, terminal technologies such as JTE and FLR widely used in Si and SiC devices are difficult to implement in vertical GaN devices. Therefore, there is an urgent need to develop effective terminal protection technologies and processes suitable for GaN devices to reduce reverse leakage current and increase withstanding voltage.
- Dynamic characteristics and long-term reliability: Research on the dynamic performance, surge capability, avalanche capability, and device

lifetime of vertical GaN p-n diodes is still in its infancy, and further experimental verification is needed.

- Cost: GaN substrate costs are still high, further reducing device materials and manufacturing costs remains an important challenge.

➢ Potential solution:

- Study high-doping p-GaN epitaxial technology, optimize ohmic contact process of p-GaN, reduce ohmic contact resistance, and reduce the forward voltage drop of vertical GaN p-n diode.
- Use a new terminal structure design, explore the etch isolation process with low damage and junction leakage, study terminal structures such as ion implantation JTE, field limiting ring, mesa combined field plate, develop efficient terminal protection technology for GaN devices, suppress electric field concentration in the edge of the Schottky device junction, increase the withstanding voltage.
- Conduct GaNp-n diode dynamic performance test, optimize device reverse recovery time, junction capacitance parameters. Conduct avalanche capacity, surge capacity, aging, and other reliability tests to evaluate the long-term reliability of devices.
- The development of large-size GaN single crystal substrates and substrate engineering technology helps to further reduce the cost of vertical GaN devices.

1.3.4.3 Vertical GaN transistor

➢ Development trend:

- Vertical GaN transistors can be mainly divided into two types: current aperture vertical electron transistor (CAVET) and trench MOSFET (as shown in Figure 28 [10]).
- CAVET devices can retain 2DEG, but the implementation of p-GaN current blocking buried layer is difficult, requiring multiple etching and epitaxial regrowth, and the preparation of material and device is complex, also, threshold regulation is not easy.
- Materials and device fabrication of trench MOSFET which is natural normally-off devices is relatively simple, and it is predicted to become mainstream vertical GaN transistor technology.
- The trench MOSFET gate dielectric materials mainly include AlN, SiNx, SiO_2, etc., and the growth processes include plasma enhanced chemical vapor deposition (PECVD), metal organic chemical vapor deposition (MOCVD), and atomic layer deposition (ALD). MOS interface characteristics of trench gate region have an important impact on threshold voltage and device stability.
- At present, the breakdown voltage of GaN trench MOSFET is 1.2kV~1.7kV, and the on-resistance is 1.5 mΩ·cm2~2.0 mΩ·cm^2. It is

expected that the breakdown voltage can reach 3.3kV in 2025~2030, reach 4.5kV in 2025~2030.

- At present, manufacturers have adopted vertical GaN Schottky diodes and vertical trench gate MOSFET to fabricate DC-DC converters based on vertical GaN devices. However, the technology is still in the research and development stage, and its industrialization still needs to overcome cost and reliability challenges.

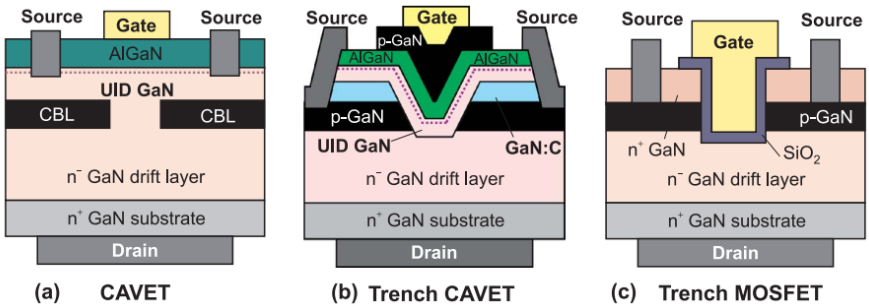


Fig 1.28 Structure diagram of the GaN transistor

➢ Challenge:

- GaN trench MOSFET faces challenges such as low channel electron mobility and high threshold controlling, which are mainly related to the interface properties of the gate dielectric and etched GaN.
- There is usually a large amount of interface charge on the interface of the gate dielectric and the GaN after etching, which causes problems of threshold voltage drift, reverse characteristics, and poor switching characteristics.
- Dynamic characteristics and long-term reliability: Research on the dynamic performance, surge capability, avalanche capability, and device lifetime of vertical GaN p-n diodes is still in its start stage, and further experimental verification is needed.
- Cost: GaN substrate costs are still high, further reducing device materials and manufacturing costs remains an important challenge.

➢ Potential solution:

- Use channel layer regrowth, MOS interface optimization, and gate dielectric deposition process optimization to improve channel mobility and reduce device channel resistance.
- Develop low-damage GaN gate trench etch technology, study damage repair methods such as surface treatment and annealing after etching, reduce trap charge on the interface of gate dielectric and GaN after etching, enhance device stability.
- Conduct GaN transistor switching characteristics and dynamic performance tests to extract junction capacitance parameters. Conduct avalanche, BTI, TDDB, and other tests to evaluate the long-term reliability of devices.
- The development of large-size GaN single crystal substrates and substrate engineering technology helps to further reduce the cost of vertical GaN

devices.

1.3.5 Diamond materials and devices

1.3.5.1 Diamond epitaxy

- Development trend: (as shown in Fig 1.29, Fig 1.30)
  - The continuous advancement of CVD technology and the continuous breakthrough of key technologies in heteroepitaxial growth have led to the continuous reduction of material epitaxy costs.
  - The Si-based heteroepitaxial dedicated single crystal diamond substrate for semiconductor devices is expected to reach 6 inches in 10-15 years and exceed 8 inches in the next 20-30 years. The homoepitaxial high-quality single crystal diamond substrate is expected to break through 3 inches while reducing costs, as shown in Fig1.29.
  - In the case of gradually mastering the mechanism of diamond heteroepitaxial nucleation, breakthroughs will be made in the defect control technology of heteroepitaxial single crystal diamond, and the epitaxial quality of the material will be continuously improved so that the quality of the heteroepitaxial single crystal diamond will be close to the quality of homoepitaxial.
  - The defect density of the heteroepitaxial single crystal diamond is expected to reach 106 cm^{-2} in 10-15 years and 105 cm^{-2} in 2040, as shown in Fig 1.30.
- Challenge:
  - Uniformity and stress of homoepitaxial large-area diamond.
  - Nucleation and defect regulation of heteroepitaxial.
  - Uniformity of large-scale epitaxy.
  - Stress regulation of large-scale epitaxy.
- Potential solution:
  - In-situ monitoring of stress during epitaxial growth, adjusting growth parameters in time to adjust stress.
  - During epitaxial growth, the substrate rotates and revolves simultaneously to improve growth uniformity.
  - Study heteroepitaxy nucleation mechanism and stress regulation, modify growth parameters.
  - Accurate model of the effects of growth parameters, microwave distribution, cavity, and sample stage should be established to adjust the structure of the device.

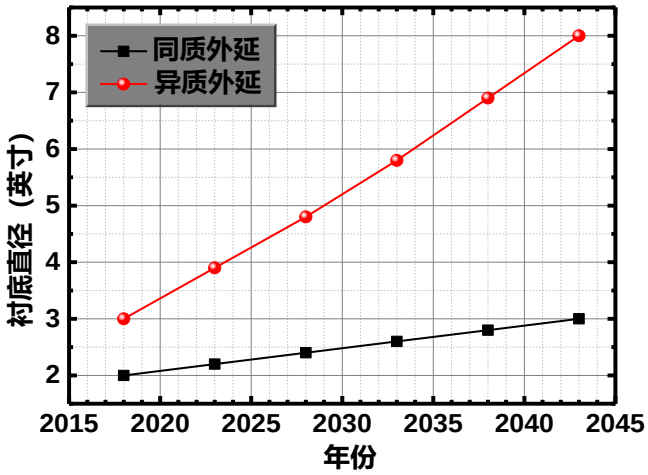


Fig 1.29 Development trend of the size of the diamond substrate

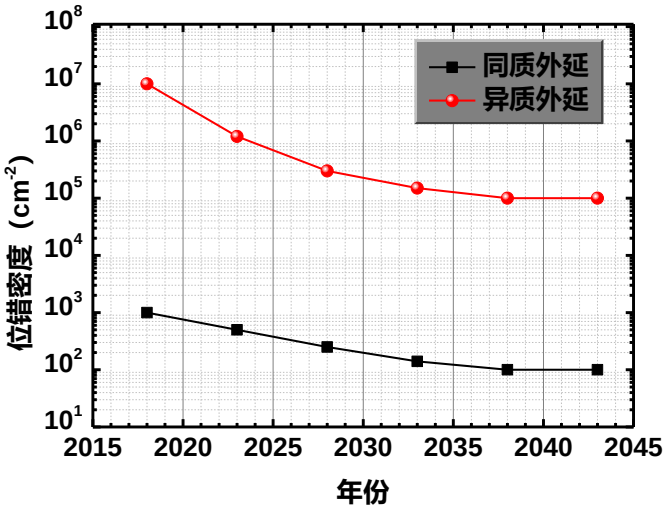


Fig 1.30 Development trend of diamond substrate defect density

1.3.5.2 Diamond electronic device

1.3.5.2.1 Diamond power electronic device

- **Withstand voltage level of device**

➢ Development trend:

- The withstanding voltage level of diamond hydrogen terminal power electronic devices is expected to increase from the current 3MV/cm to 7MV/cm in the next 5-10 years, and then will be in a stable state, mainly due to the two factors: one is device manufacturing technology, the other is the market of hydrogen-terminal diamond.
- In terms of the market, it is expected that with the continuous improvement of capabilities of the diamond power electronic device, the

capabilities of existing GaN and SiC devices will be reached or exceeded, and with the breakthrough of homoepitaxial substrate technology, the cost will be reduced, then it will achieve a certain market share.

- Challenge:
  - Technical aspects: Under higher electric field, the diamond hydrogen terminal may reach the critical breakdownelectric field, and there is a mutual constraint between the breakdown voltage and the current density of the diamond device, so it is necessary to develop a new device process or look for new conductive mechanisms to increase the breakdown voltage while maintaining current density. There is an instability problem in the hydrogen terminal conduction of the diamond surface, which will affect the long-term reliability. It is necessary to find a suitable passivation scheme to ensure the stability of the device.
  - Market: With the continuous optimization of R&D and production control of GaN and SiC power electronic devices, the cost will be reduced. However, due to the cost of diamond substrates, it is difficult for diamond power electronic devices to break through in the mainstream application market of 1200 V and below.
- Potential solution:
  - To carry out research on diamond vertical devices, it is necessary to increase the thickness of the epitaxial layer to increase the withstanding voltage in the vertical direction, optimize the field plate structure, regulate the electric field distribution, to realize the devices that meet the ultra-high voltage and high-power applications. Achieve a dominant position in the field where traditional GaN and SiC devices are difficult to achieve to realize market dominance.

■ **Device current density**

- Development trend:
  - Considering the optimization process and controlling the cost, the new doping technology is developed to improve the carrier mobility and areal density, thereby increasing the output current density of the device and reducing the on-resistance. In the next 30 years, the existing output current density will be doubled to 2A/mm.
  - Market: Single crystal diamond is extremely high in thermal conductivity and good in heat dissipation. It is very suitable for high-power device applications. With the improvement of diamond device performance and cost reduction, it is expected to gradually occupy the market in the field of ultra-high power devices in the next 30 years.
- Challenge:
  - It is necessary to develop a new transfer doping mechanism for the hydrogen terminal diamond’s surface to form a stable and high carrier mobility layer to improve device performance.
  - The size of the device's field plate for withstanding voltage and the reduction of the spacing between the electrodes pose a high challenge to

device reliability.

- Potential solution:
  - Look for new types of transfer doping media, doping methods, etc.
  - Increase investment in reliability to establish failure model and device lifetime dependence on device size and defect density.

1.3.5.2.2 Diamond microwave power diode

- Development trend:
  - Single crystal diamond has the advantages of high crystal quality, high carrier mobility, and good substrate insulation. It is especially suitable for making microwave power diodes with high conversion efficiency, high breakdown electric field, low leakage, and high current density. Due to the ultra-high thermal conductivity of diamond, it is expected that in the next 30 years, the diamond-based microwave power diode will achieve an absolute value of turn-on voltage of less than 1V, the forward current is 100mA @2.5V, the reverse breakdown is greater than 200V, and the operating frequency is reached 3GHz.
- Challenge:
  - Bulk doping of diamond has low activation efficiency, poor conductivity, and ohmic contact resistance is difficult to reduce, resulting in high device turn-on voltage and low current density.
  - A diode-based on termination of diamond surfaces with hydrogen, although ohmic contact is easy to fabricate, carrier mobility is low, the frequency characteristic is poor, the device output current is small, and reliability is poor.
- Potential solution:
  - Thin-layer heavy doping and new ohmic contact metal for good ohmic contact, to reduce ohmic contact resistance and improve device characteristics.
  - Look for new transfer doping media to improve the conductivity of the diamond surface, find suitable Schottky metals to reduce capacitance and improve device microwave characteristics.

1.3.5.2.3 Reliability of diamond electronics

- Development trend:
  - The downstream industry of chip has strict requirements on device reliability, due to the diamond as alternative new materials and new products. This is another important factor that restricts the development of diamond device market in addition to cost performance.
  - GaN and SiC device suppliers have carried out different levels of

reliability testing. The published data indicates that the device can work reliably for a long time. The diamond-based device also needs to be tested accordingly, and a corresponding set of test and classification standards are developed to verify its work stability.

- In the next 30 years, with the development of diamond materials and devices, the market share will continue to increase, and for a variety of application needs, a series of corresponding test standards will be released to meet the reliability requirements of their respective applications.

➢ Challenge:

- At present, diamond devices are still in the development stage and have poor reliability, also, they lack reliability data for extension, device, package, test, etc.

➢ Potential solution:

- The failure model under each acceleration condition is established and verified based on the overengineering of epitaxy, device, package, test, and integrating the existing reliability data of different levels. Form a complete set of diamond device reliability test standards.

1.3.5.3 Diamond nuclear detector

➢ Development trend:

- Based on the improvement of device performance, diamond nuclear detectors are developing towards large-scale, ultra-high-speed detection and application of strong radiation fields. The size of diamond nuclear detectors is expected to reach more than 1 inch in the future, and the charge collection efficiency is stable over 95%. The response time is reduced to the sub-ns level, and the device can withstand the high temperature above 400 ° C. The anti-irradiation intensity can adapt to the detection of future nuclear fusion reactors and super-radiative radiation fields, for humans to solve the mystery of the origin of the universe and develop future energy solutions.
- In terms of cost, due to the constraints of artificial growth environment, grinding process, and market monopoly, the price of the electronic grade ultra-pure diamond single crystal is as high as 3,000 US dollars per piece (size 4.5mm×4.5mm×0.3mm), and the diamond nuclear detector developed by CIVIDEC has reached more than 20,000 US dollars. Therefore, vigorously developing artificial growth technology to break the monopoly can effectively reduce the cost of devices.
- In terms of market, DE BEERS's electronic grade ultra-pure diamond single crystal has a market share of nearly 100%. The only manufacturer that can commercialize diamond nuclear detectors is CIVIDEC. Since the market data of the two companies are not disclosed, the market value cannot be accurately estimated at present. With reference to the market

value of silicon-based devices, the market value of diamond detectors is expected to reach tens of millions of dollars.

- Challenge:
  - Because diamond has a small atomic number, the absorption of nuclear radiation is not as good as that of the high atomic number. Therefore, how to improve the sensitivity of the diamond detector is a major technical problem.
  - The bandgap of diamond is large (5.45eV), so it is difficult to form a good ohmic contact, and the adhesion between diamond and metal is poor, so the ohmic contact problem is also a key factor restricting the development of diamond nuclear detectors.
  - The transport polarization effect after nuclear radiation affects the performance of the detector, and it is important to reduce it.
  - Diamond nuclear detectors combined with diamond field effect transistors or other wide-bandgap semiconductor devices to form fully integrated pixel array detectors still have great difficulties.
- Potential solution:
  - Use heterogeneous composite structures to achieve energy band regulation and improve the sensitivity of diamond nuclear detectors.
  - In the heterogeneous composite structure, a material with narrow bandgap acts as the surface contact layer, and diamond acts as the detection sensitive region, which is expected to achieve excellent ohmic contact characteristics.
  - Pre-irradiation of the detector before leaving the factory to fill the charge trap center to stabilize device performance.
  - Breakthrough in diamond doping technology or construction of fully integrated pixel arrays using hydrogen-terminated surface channel-type diamond field effect transistors.

1.3.6 Ga_2O_3 epitaxy and device

1.3.6.1 β- Ga_2O_3 substrate and epitaxy

1.3.6.1.1 β- Ga_2O_3substrate

- **The size of the single crystal**
- Development trend:
  - Gallium oxide crystal (band gap 4.8 eV) is an excellent ultra-wide bandgap semiconductor material, which has the advantages of a large bandgap, high breakdown field strength, and low device loss. It will have good application prospects in low loss devices of medium and low voltage

and device miniaturization, especially in high voltage power devices.

- The diameter of the substrate currently used is mainly 10-50 mm. With the gradual improvement of the performance of β-Ga_2O_3-based power electronic devices and ultraviolet detectors, β-Ga_2O_3-based microelectronics and optoelectronic devices are rapidly industrialized. Therefore, device costs are becoming more and more sensitive. Similar to silicon, large diameter substrates can effectively reduce the cost of individual device fabrication. Therefore, large-size single crystal substrates will be the main direction of future research and development.
- At present, Tamura Corporation of Japan has realized the industrialization of a 50 mm diameter β-Ga_2O_3 substrate, but domestic is still in the research stage.
- Tamura Corporation of Japan has completed the development of 150 mm diameter β- Ga_2O_3 substrate. It is estimated that 2020, 100 mm diameter single crystal will be industrialized; before 2030, a single crystal with a diameter of 150-200 mm will become the mainstream.

➢ Challenge:

- The design and implementation of temperature field:
  A suitable temperature provides a stable environment for the crystallization process and is the basis for the preparation of β-Ga_2O_3 single crystals. The crystal quality and shape control are directly related to the temperature field. Unsuitable temperature fields can lead to problems such as difficulty in crystal, low crystal quality, crystal cracking, and unstable crystal diameter. Therefore, to grow high-quality crystals, we must design a reasonable temperature field.
- Protection of noble metal crucible during the growth of large-sized single crystals:
  The β-Ga_2O_3 melt undergoes a decomposition reaction at a high temperature, and the product forms an alloy with the crucible, which in turn causes loss of the crucible. How to suppress the decomposition ofGa_2O_3while preventing the oxidation of noble metals is a key issue in the growth of large crystals.
- Large size single crystal crack control in shoulder growth progress:
  There are two cracking planes in the β-Ga_2O_3 crystal, and the crystal is prone to cracking. Defects or stresses in the shoulder formation process can cause twinning or cracking. How to improve the quality of the seed, reasonable control of the shoulder growth process and inhibit the cracking of the crystal in shoulder growth progress is another key problem that needs to be solved in the process of increasing the size of the substrate.

➢ Potential solution:

- The numerical simulation results are used to guide the design of temperature field of large-size single crystal; optimize the protective atmosphere, seeding and shoulder growth process to achieve the growth of high-quality and large-size single crystal.

■ **Crystal defect density**

➢ Development trend:

- With the development of high-voltage, high-power β-Ga_2O_3-based power electronic devices, the requirements for device quality are getting higher and higher. Defects in the substrate (eg, nanotubes, screw dislocations, twins) can negatively affect device performance. Therefore, in the future, it is necessary to reduce the defect density in the substrate by optimizing the temperature field and growth of neck technology.
- At present, the reported defect density of β-Ga_2O_3 is mostly at the level of 104-105 cm^{-2}, and the next step defect density will gradually develop to the level of 10^3 cm^{-2}.

➢ Challenge:

- Cost:

  In order to reduce the defect density in the crystal, it is necessary to optimize the crystal growth process, increase the neck length and reduce the crystal growth rate, which will increase the substrate cost.

➢ Potential solution:

- Analyze the generation and extension mechanism of defects, theoretically guide the method of reducing the defect density; optimize the crystal growth equipment, improve the mold structure and surface quality, explore the seed crystal and growth of neckin different directions, and reduce the defect density in the crystal.

■ **Substrate process**

➢ Development trend:

- Bulk monocrystalline crystals need to be processed by orientation, cutting, grinding, polishing, etc. before they can be applied to the fabrication of semiconductor devices. Unlike Si single crystal and sapphire, the β-Ga_2O_3 crystal is a typical hard and brittle material, which is easy to cleave and difficult to process. Therefore, the processing technology of large-size β-Ga_2O_3 crystals needs to be developed.
- At present, the processing technology of the substrate in different directions of the β-Ga_2O_3 crystal is not mature. Japan has obtained the industrialization of a 50 mm diameter β-Ga_2O_3 substrate by chemical mechanical polishing. The State Key Laboratory of Crystal Materials of Shandong University, China, obtained the mechanical stripping technology for the first time in the world and obtained a high-quality single crystal substrate in one step. But CMP processing technology for large-size substrates is still in the research stage.
- With the increasing size of single crystals and the development of crystal processing technology, it is estimated that by 2020, the processing technology of 100 mm diameter substrate will become the mainstream; before 2030, substrates with a diameter of 150-200 mm will enter the market.

➢ Challenge:

- Processing cracking:
  There are two easy-cleavage surfaces in the β-Ga_2O_3 crystal, which are prone to cracking under the action of large external force. Therefore, β-Ga_2O_3 crystals are prone to break during cutting and grinding.
- Damage of substrate surface:
  The substrate will produce a large amount of surface damage during the cutting and grinding process. The debris generated by the cleavage during the polishing process will also cause scratches on the surface of the wafer, and the presence of the damaged layer or scratch will seriously affect the performance of the device. Therefore, how to eliminate the surface damage layer and surface scratches is a key issue in the processing of β-Ga_2O_3 crystals.

➢ Potential solution:

- Explore ways to optimize crystal cutting to reduce damage during crystal cutting and prevent crystal cracking; optimize chemical mechanical polishing of large-size β-Ga_2O_3 crystals, explore suitable polishing fluids, polishing pads, and combine chemical and mechanical grinding to eliminate surfaces damage layer and surface scratches.

1.3.6.1.2 Ga_2O_3 epitaxy

■ **Epitaxy technology**

➢ Development trend:

- Molecular Beam Epitaxy (MBE): MBE is mainly used for homoepitaxial growth of MOSFET devices. The grown β-Ga_2O_3 film has the advantages of good crystal quality, smooth surface, and controllable electron concentration. It is the main homoepitaxial growth of β-Ga_2O_3, and the high-quality $(AlGa)_2O_3/Ga_2O_3$ heterojunction grown by MBE, can realize the two-dimensional electron gas generated by modulation doping.
- Metal Organic Chemical Vapor Phase Epitaxy (MOCVD): MOCVD can be used for homoepitaxial growth of MOSFET device structures. In addition, MOCVD can also be used for heteroepitaxial growth of Ga_2O_3 films; in heteroepitaxial, by adjusting the appropriate growth temperature, gas pressure, the VI/III ratio can control the Ga_2O_3 film of α phase, β phase, and ε phase; MOCVD uses trimethylgallium (TMGa) and triethylgallium (TEGa) to achieve a growth rate of several micrometers per hour, and realize the control of electron concentration by doping.
- Halide vapor phase epitaxy (HVPE): In the case of homoepitaxy where a thick film is required, HVPE is commonly used, and its speed can even be as high as several tens of micrometers per hour. However, high-quality HVPE film growth generally requires speed control of several micrometers per hour; HVPE is currently used for homoepitaxial growth of SBD devices.

- Mist chemical vapor deposition (mistCVD): For α-Ga_2O_3 and sapphire (α-Al_2O_3) has the same characteristics of corundum structure, mistCVD technology is mainly used for heteroepitaxial diffusion of α-Ga_2O_3 film on the sapphire substrate. It is the most effective means to realize heterojunction growth of Ga_2O_3, alloys, including α-$(AlGa)_2O_3$ alloy, α-$(InGa)_2O_3$ alloy, α-Ir_2O_3/α- Ga_2O_3 heterojunction, etc.. α- Ga_2O_3 grown on sapphire substrate has reached the requirements of SBD device application and can be transferred to the copper substrate by the substrate stripping technology, which effectively improves the heat dissipation of the α- Ga_2O_3 based device.

➢ Challenge:

- MBE: Low growth rate, its growth rate is much lower than other epitaxial technologies such as MOCVD, HVPE, etc., greatly increasing the epitaxial cost.
- MOCVD: The process of MOCVD growth of Ga_2O_3 film is still immature, and the crystal quality of β-Ga_2O_3 homoepitaxial film is not as good as MBE.
- HVPE: The β-Ga_2O_3 homoepitaxial film has a high surface roughness and needs to be polished after growth.
- MistCVD: The quality of the heteroepitaxial α-Ga_2O_3 film is not as good as β-Ga_2O_3 homoepitaxial film.

➢ Potential solution:

- Develop MOCVD heteroepitaxial technology, especially heteroepitaxial technology based on the silicon substrate, to reduce the cost ofGa_2O_3 film.
- Further optimize the MOCVD homoepitaxial growth process based on the β-Ga_2O_3 substrate, including increasing the film growth rate, reducing the density of stacking defects and twins, inhibiting the residual of carbon and hydrogen impurities, and improving the crystal quality of the film.

■ **Homoepitaxy**

➢ Development trend:

- At present, β-Ga_2O_3 homoepitaxial is still dominated by MBE, but MOCVD has begun to be used for homoepitaxial extension of MOSFET device structure. HVPE has also been gradually used for homoepitaxial extension of SBD device structure.

➢ Challenge:

- At present, the cost of β-Ga_2O_3 single crystal substrate is still much higher than that of sapphire, silicon, etc., and is limited by the size of β-Ga_2O_3 single crystal substrate. At present, the homoepitaxial growth of β-Ga_2O_3 generally does not exceed 50mm.
- The realization of hole conduction has been a material fabrication problem for many oxide semiconductors. At present, for the growth of β-Ga_2O_3homoepitaxial films, hole conduction has not been achieved.
- At present, MOCVD and HVPE have failed to achieve the growth of multi-alloys and heterojunctions.

- Since the atomic bond energy of β- Ga_2O_3 along the <100> crystal orientation is weak, it is easy to form high-density stacking defects and twins along the (100) plane during homoepitaxial growth.

➢ Potential solution:

- Introduce a suitable aluminum-containing, In-containing metal organic source, and optimize the MOCVD growth process to achieve the growth of multi-alloy and heterojunction.
- Exploring the influence of homogeneous substrates with different crystal planes and different tilted cutting angles on the formation of defects during epitaxial growth, and selecting suitable homogeneous substrates for epitaxial growth.

■ **Heteroepitaxy**

➢ Development trend:

- Ga_2O_3 includes five phases: α, β, γ, δ, and ε. Among them, β-Ga_2O_3 is a stable phase, α- Ga2O3 and ε-Ga_2O_3 are metastable phases, and γ phase and δ phase are poor in stability. The β phase is a monoclinic system, and there are fewer heterogeneous substrates available. Therefore, β-Ga_2O_3 is not suitable for heteroepitaxial growth; both the α phase and the ε phase have hexagonal symmetry, and it is suitable to use a substrate having hexagonal symmetry, such as sapphire or silicon (111) surface substrates. At present, the heteroepitaxial growth of Ga_2O_3 film mainly adopts sapphire substrate, which is beneficial to realize large-scale and low-cost preparation of Ga_2O_3 film. If the silicon (111) plane can be used for heteroepitaxial growth, the compatibility of the Ga_2O_3 based device with the existing semiconductor process can be further improved.
- On a variety of hexagonal symmetry substrates such as sapphire, film formation of ε-Ga_2O_3 is generally observed by MOCVD heteroepitaxial growth. Due to the spontaneous polarization effect in ε-Ga_2O_3, the experience of forming two-dimensional electron gas in AlGaN/GaN can be used to form a high mobility two-dimensional electron gas in the ε-Ga_2O_3based heterojunction to solve the problem of low mobility of Ga_2O_3 material.
- At present, the growth of high-quality α-Ga_2O_3 film is realized by mistCVD epitaxial technology, and an SBD device with on-resistance of 0.1 $m\Omega cm^2$ is prepared. Since both α-$Ga_2O_3$and sapphire (α-Al_2O_3) have a corundum structure, and the sapphire substrate is inexpensive. Therefore, α-Ga_2O_3 heteroepitaxial growth is expected to become the main means of preparation of high current, low-cost SBD devices.
- α-Ir_2O_3 is easy to realize hole conduction and has a small lattice mismatch with α-Ga_2O_3. Therefore, heterojunction based on α-Ir_2O_3/α-Ga_2O_3 may be one of the means to compensate or replace p-type α-Ga_2O_3.
- Ga_2O_3 based materials generally have low thermal conductivity, which severely limits the application of Ga_2O_3 based devices in high power applications. Substrate stripping and transfer have been achieved based on

the α- Ga_2O_3 heteroepitaxial sapphire substrate. Therefore, heteroepitaxial bonded substrate stripping transfer technology will become an effective means to solve the heat dissipation problem of Ga_2O_3 devices.

- Challenge:
  - Due to the heteroepitaxial growth, the crystal quality of α-Ga_2O_3 and that of ε-Ga_2O_3 films is not as good as homoepitaxy, and the corresponding device performance is also limited.
  - α-Ga_2O_3 and ε-Ga_2O_3 belong to the metastable phase, the preparation temperature is generally 400℃~700℃, so the stability of the α-Ga_2O_3 based device still needs further research.
  - At present, the growth of α-Ga_2O_3 and ε-Ga_2O_3 heteroepitaxial films has not yet achieved hole conduction.
- Potential solution:
  - In the process of the epitaxial α- Ga_2O_3 film by mistCVD or epitaxial ε-Ga_2O_3 film by MOCVD, two-step or multi-step growth method is introduced to control the stress and defects in the heteroepitaxial process and improve the crystal quality of the Ga_2O_3film.

1.3.6.2 Ga_2O_3 power device

1.3.6.2.1 Ga_2O_3-based SBD

■ **β- Ga_2O_3-based SBD**

- Development trend:
  - With the use of HVPE for β-Ga_2O_3 homoepitaxial epitaxy in recent years, the preparation of β-Ga_2O_3-based SBD has made great progress. As far as the current Ga_2O_3 epitaxial technology is concerned, HVPE will become the main homoepitaxy of β-Ga_2O_3-based SBD in the future.
  - Using the mistCVD heteroepitaxial technology, combined with substrate stripping and transfer to improve device heat dissipation, it can achieve α-Ga_2O_3-based SBD withstand voltage above 800V, and the on-resistance is as low as 0.1mΩcm^2. The α- Ga_2O_3 based SBD based on the TO220 package has launched the first commercialized product in 2017. The future α-Ga_2O_3 based SBD will be suitable for medium and low withstanding voltage and high current applications.
- Challenge:
  - At present, Ga_2O_3-based MOSFET devices generally suffer from high source-drain contact resistance.
  - At present, the breakdown voltage of Ga_2O_3-based MOSFET devices is generally low, and the breakdown resistance is still far from fully exploiting the potential of wide-band Ga_2O_3 materials.
  - During the preparation of Ga_2O_3-based MOSFET devices, especially

during the preparation of normally-off devices, the interface damage caused by dry etching of the channel is easy to form a defect state, resulting in drift of the turn-on voltage.

- Normally-off Ga_2O_3-based MOSFETs generally face a problem of large forward turn-on voltage (several volts to tens of volts), mainly due to excessive access region resistance and source-drain contact resistance.
- A normally-on Ga_2O_3-based MOSFET improves the channel doping electron concentration, which reduces the on-resistance of the device and increases the saturation current, but is more difficult to turn off.

➢ Potential solution:

- Optimizing the metal type of the source and drain electrodes, the preparation process and the annealing process of the contacts can reduce the source-drain contact resistance. In addition, the use of a conductive oxide (such as indium tin oxide) as an electrode also helps to reduce the contact resistance. Further, a combination of a conductive oxide and a metal can be used as the source and drain electrode.
- Optimize the growth process of MOCVD homoepitaxial growth, reduce the defect density of β-Ga_2O_3 epitaxial layer, and improve the withstand voltage characteristics of MOSFET.
- The modulation doping $(AlGa)_2O_3$/ Ga_2O_3 heterojunction is used as the channel, and the two-dimensional electron gas transmission in the channel is utilized to reduce the on-resistance of the MOSFET device.

1.3.6.3 Ga_2O_3RF device

➢ Development trend:

- β-Ga_2O_3 has the characteristic of high critical breakdown electric field and high saturated electron velocity. Therefore, the short channel can be used to improve the operating frequency of the RF device while ensuring that the device is not broken down. Currently, the MOCVD homoepitaxial growth is used to achieve RF devices with the cutoff frequency and maximum oscillation frequencies of 3.3 GHz and 13 GHz, respectively.

➢ Challenge:

- In the case of high power and large voltage operation, the RF device is very easy to fail, mainly due to poor heat dissipation of the device.

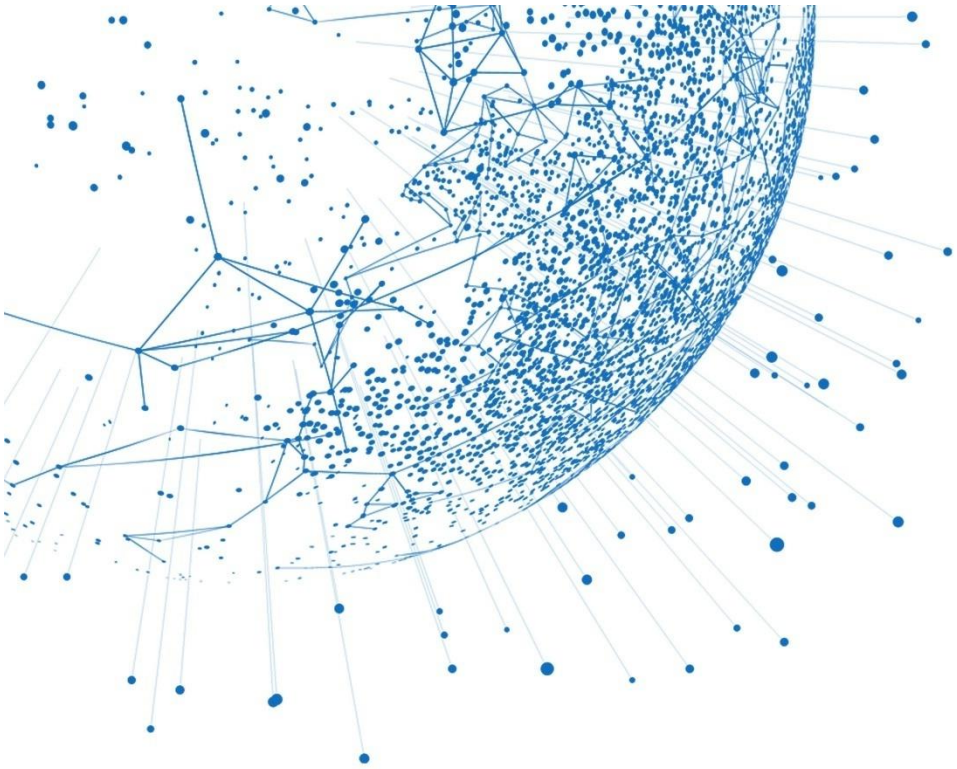
➢ Potential solution:

- Optimize device size.
- Reduce the operating temperature of the device by means of substrate thinning and substrate heat dissipation.

1.4 Summary

The third generation of power electronic devices represented by SiC and GaN cater to the needs of the power electronics market below tens of kilowatts for high conversion efficiency, high system integration, high cost performance, and extreme use environment. With the growing popularity of its application, technology, cost, reliability has evolved. In the next 30 years, the main development trends are as follows:

- Substrate and epitaxy: The diameter of the substrate will continue to develop in the direction of large diameter. The proportion of large diameter substrate will increase continuously; the density of defects in the substrate will decrease continuously, and the density of TSD and BPD will be reduced to lower than $10/cm^2$; the defect density in epitaxy will also drop significantly; due to the increasing diameter of the substrate and the available thickness of the single crystal, the unit price of the substrate will decrease in the next 30 years.
- Devices: The chip of the device will be more miniaturized and intelligent, the device current density will be greatly increased, the current/voltage class will continue to increase, and the cost of the device will gradually approach the Si device.
- Packaging: Advanced, new, working in high-temperature packaging processes will be gradually applied to the packaging process of devices, reducing package parasitic parameters, optimizing package heat dissipation characteristics, so that the advantages of materials and devices will be better to play.
- Reliability: The possibility of using SiC devices in the future high-end industrial fields and military, aerospace, ships, weapons and other fields in the extreme environment will increase gradually. The improvement of reliability will promote the marketing of SiC power devices.



Packaging and Module

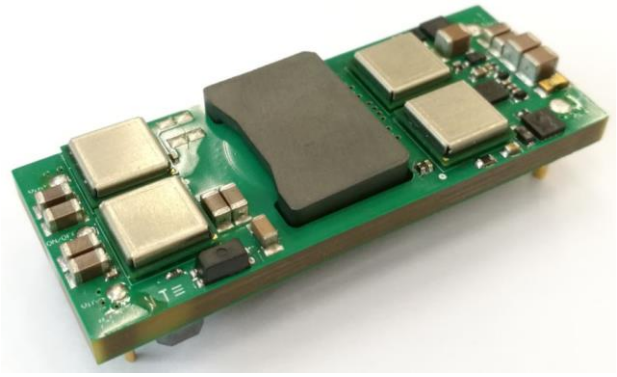
2.1 Background

Packaging and module play an important role between device and system. While the application of Wide Bandgap semiconductor is arising, it is predicted that, the recent packaging and module technology of Wide Bandgap semiconductor do not have major difference compared to that of Si-based semiconductor. However, since the application of Wide Bandgap semiconductor becomes more popular and be widely used, a different development roadmap on the packaging and module technology of Wide Bandgap semiconductor will be derived in the future 20~30 years. The development trend of packaging and module technology of Wide Bandgap semiconductor will be driven towards lower loss, lower inductance, higher power density, higher heat dissipation, higher integration, multi-function, etc.

This technology roadmap provides the development trend of packaging and module technology of Wide Bandgap semiconductor in future 30 years (2018~2048), from the perspective of structure & dimension, electric performance, power & heat dissipation, material & process, and reliability. In each category, the roadmap proposes 2 kinds of module products which will immediately apply Wide Bandgap semiconductor devices and have huge market size, i.e. DC-DC converter and MOSFET module. These 2 module products can be applied to the industries those have great potential and progress, while the Wide Bandgap semiconductor can facilitate the development of them. Therefore, these 2 module products were selected with greater research and reference value.

2.2 Product Definition

- DC-DC Convertor: It is mainly applied to telecommunication, server, network, data storage, industrial, military and other industries (the typical structure is shown in Fig. 2.1). Generally, it is connected between AC-DC converter and non-isolated point-of-load (POL) power module. The DC-DC converter mentioned in the roadmap primarily adopts GaN devices and mostly designed as brick. The input voltage is normally 24~380V, and the output voltage is normally 2.5~12V, the power level is usually below kilowatts.



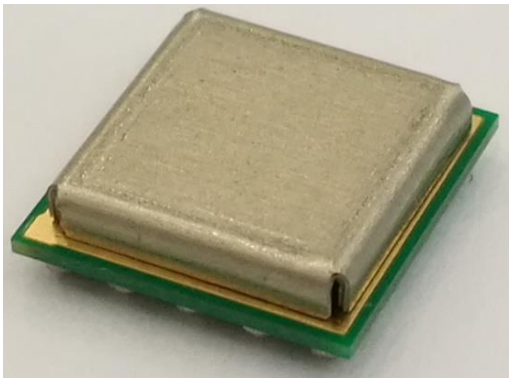


Fig. 2.1 Typical structure of DC-DC converter adopting GaN device

- MOSFET Module: It is integrated in DC-AC inverter, and mainly used in motor drive, traction and dragging, home appliance, cooling fan and lighting industries (the typical structure is shown in Fig. 2.2). Generally, it is connected with DC power source, battery, AC-DC rectifier or DC-DC transducer, and motor loading or three-phase inductive loading. The MOSFET module mentioned in the roadmap primarily adopts SiC devices and mostly integrated in inverter. One of the major applications of MOSFET modules are in-vehicle motor drive with box-based inverter. The input voltage is normally single-phase 300~700V, and the output voltage is normally three-phase 100~250V. The output frequency is 0~400Hz and the power level is 20~300kW.

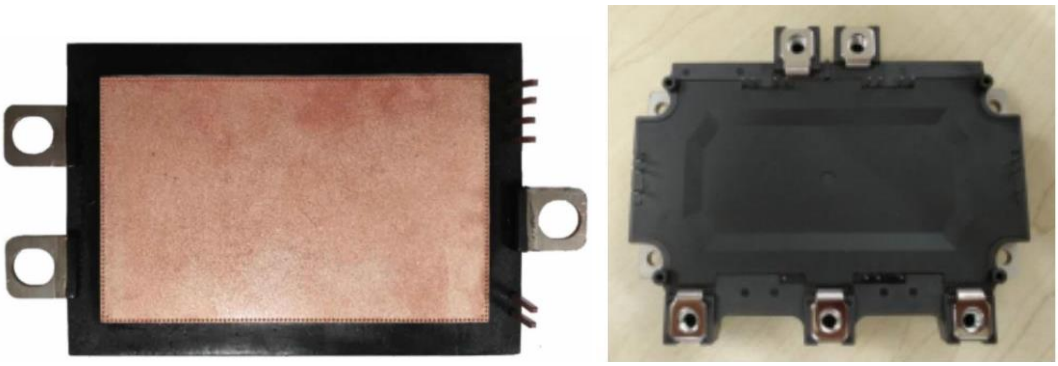


Fig.2.2 Typical structure of MOSFET adopting SiC device

2.3 Overview of Driving Force

- Market: The power devices is gradually modularized and the global market size is growing year by year. The market size in China is even expanding faster since the starting point is relatively low.
- Cost: The unit cost of power module decreases year by year. In the recent years, the modules using Wide Bandgap semiconductor are more expensive than that using Si-based semiconductor. However, the overall cost of the entire system is lower owing to the excellent performance of Wide Bandgap semiconductor.
- Integration Density: The integration density is gradually increasing, and

evolving from 2D planar integration to 3D integration.

- Power Density: The power density is increasing due to the multi-functionality of the module.
- Power Requirement: The power density requirement becomes higher since the power needed in the same size of module increases when more applications of Wide Bandgap semiconductor are developed.
- Current/Voltage Requirement: The current/voltage requirement of single module becomes higher, therefore, higher requirement of heat dissipation and dielectric is needed accordingly.
- Heat Dissipation: Local heat-aggregation point is commonly found in Wide Bandgap semiconductor devices, and the increasing rate of power is obviously faster than the increasing rate of power conversion efficiency. Therefore, an increase of the overall thermal power consumption of the module places high demands on the heat dissipation performance.
- Frequency: The working frequency can be remarkably improved by adopting the Wide Bandgap semiconductor, and the size of passive devices as well as the entire system can be reduced.
- Conversion Efficiency: The conversion efficiency of the module can be improved by adopting the Wide Bandgap semiconductor. However, due to the limitation of the maximum value, the conversion efficiency will not be notably improved in later stage.
- Extreme Application: The working temperature of Wide Bandgap semiconductor is higher than that of Si-based devices, thus theoretically it can be used in more extreme conditions. However, more failure modes and mechanisms were found in the device when applied in the extreme conditions, therefore the reliability of the Wide Bandgap semiconductor module should be considered before applying to these conditions.
- Lifetime: The working lifetime of the Wide Bandgap semiconductor based power module becomes higher, since the module will be applied to industrial, military and even aerospace applications.

2.4 The Trend of Key Indicators/Parameters

2.4.1 Structure and Dimension

- **DC-DC Converter**

- Trend (as shown in Fig. 3)
  - DC-DC converter has wide range of applications in telecommunication, and most of the module type are mainly open-frame power brick. The requirement of heat dissipation and reliability is getting higher and higher with the application of Wide Bandgap semiconductor. Therefore, it is believed that the application of power supply in package will gradually increase in the next 30 years and the advantages of high heat dissipation (with uniform heat dissipation surface and high thermal conductivity) and high reliability (devices protected by plastic molding) will be shown.
  - The application of 1/2 brick module with Wide Bandgap semiconductor

will decrease since the requirement of power density is increasing.

- Since the pin specification of 1/4 brick and 1/8 brick is almost the same, 1/4 brick will be gradually replaced by 1/8 brick in the future (due to increased power density).
- Since the 1/16 brick has special pin specification, it is believed that the application of 1/16 brick will gradually decrease and the 1/16 brick will be replaced by similar or smaller size fully-molded module.

➢ Barrier and Challenge

- Cost: With the miniaturization and integration of the module, the R&D cost becomes higher, and the involvement of new devices, new materials and new processes will also require higher cost.
- High Current and Power: As the power density increase, the current and power in the same size will also increase. Therefore, new challenges on heat dissipation and reliability will be raised.
- Heat Dissipation: When the power increases but the conversion efficiency remains unchanged, the thermal power loss also increases, therefore, the cost for thermal design will be higher and the module long-term reliability will be lower.

➢ Potential Solution

- By adopting the high frequency Wide Bandgap semiconductor, the conversion efficiency will be improved, the power consumption will be decreased and the size of passive components will be reduced.
- By improving the packaging integration density, the heat dissipation surface for the heat-generation devices can be provided.

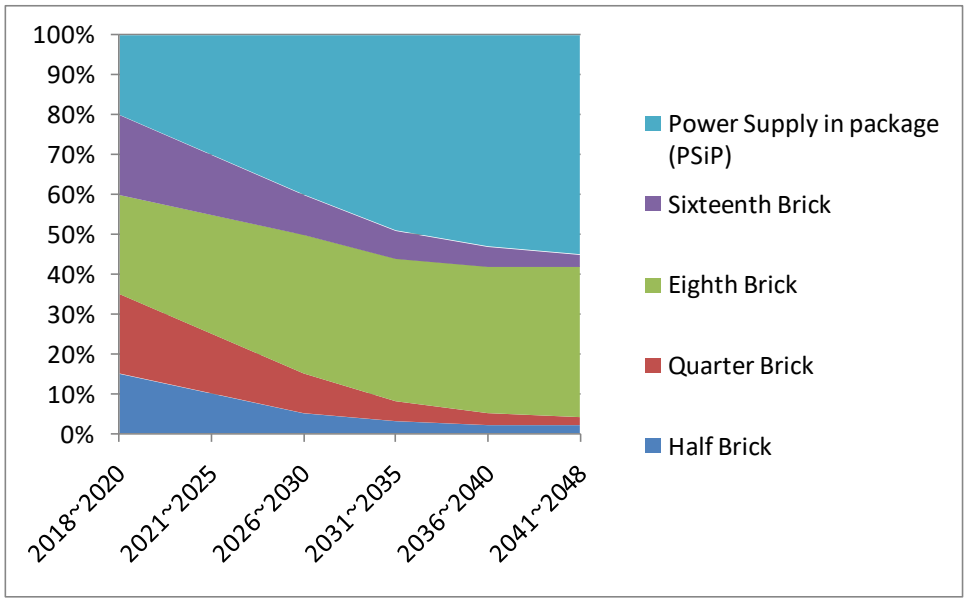


Fig.2.3 The application trend of DC-DC converter of various dimensions

■ **MOSFET Module**

➢ Trend (as shown in Fig. 2.4)

- Higher current density normally shows in SiC devices as compared to Si-based devices. The volume of SiC power module will be smaller than Si-based IGBT module under the same power level. The experts

emphasized one of the advantages of SiC power devices is the miniaturization of the packaged module. By taking Intelligent Power Module (IPM) as an example, the volume can be reduced to 2/3 or even 1/3 of the original volume of Si-based power module by using the SiC devices. The switching frequency can be 10 times higher than that of Si-based IGBT module if the high-speed switching frequency reaches to 100kHz or above. The cost of the entire system can be cut down by increasing the switching frequency and decreasing of the volume of inductors and capacitors.

- The high density packaging technology of SiC power module will be an inevitable trend, due to its high temperature and high frequency characteristics of SiC devices. The so-called high density packaging aims to provide higher power within limited volume. Firstly, the output power of SiC module should be increased (i.e. high voltage and current). Secondly, the packaging size should be reduced and the heat dissipation can be integrated by optimizing the module design (for example, double-side planer packaging). Therefore, the packaging size of SiC power module will be reduced gradually, and thus the requirement of electronic device miniaturization can be achieved.

➢ Barrier and Challenge

- The non-customized SiC power modules still adopt the Si-based packaging technology, due to the small size of the market.
- Since the generally low dielectric strength of the molding materials, sufficient insulation area is needed for high voltage SiC device packaging, resulting in larger package size.

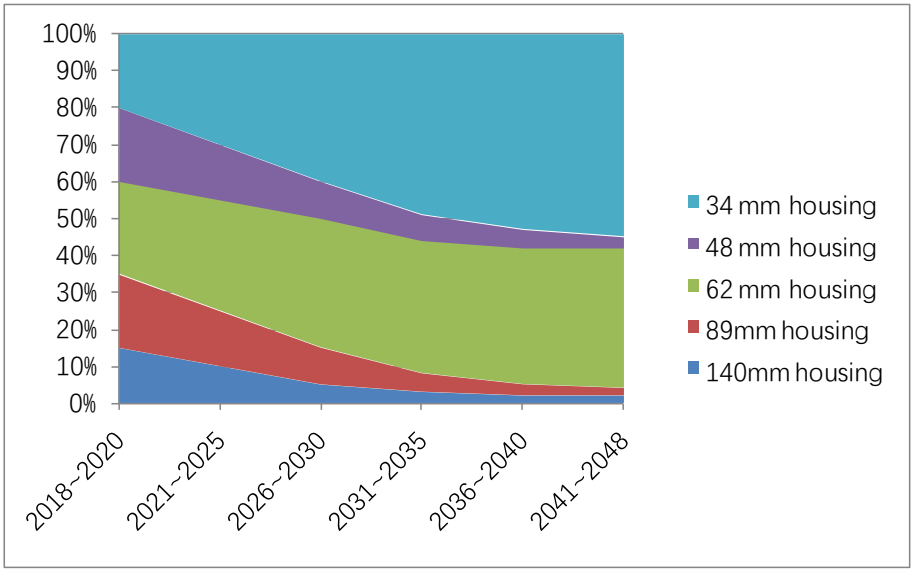


Fig. 2.4 The dimension trend of SiC-MOSFET in inverter for motor driving application

2.4.2 Electrical Performance

■ **DC-DC Converter**

- Trend of Topology Development (as shown in Fig. 2.5)
  - The LLC resonance topology will have wider application, owing to its low cost, high conversion efficiency and high packaging density.
  - The phase-shifted soft switched full-bridge topology will be widely used, since the application of wide range input and output will be more common.
  - The other current common topology will gradually vanish in the Wide Bandgap semiconductor power module. According to literature review, some of the new topologies that are still under research will enter important position, and may become the main direction in the future power module design.
- Barrier and Challenge
  - The combination with high conversion efficiency and low cost is a major challenge in the research of novel topology design for Wide Bandgap semiconductor.
- Potential Solution
  - The improvement of the conversion efficiency will be the new direction of the topology design.

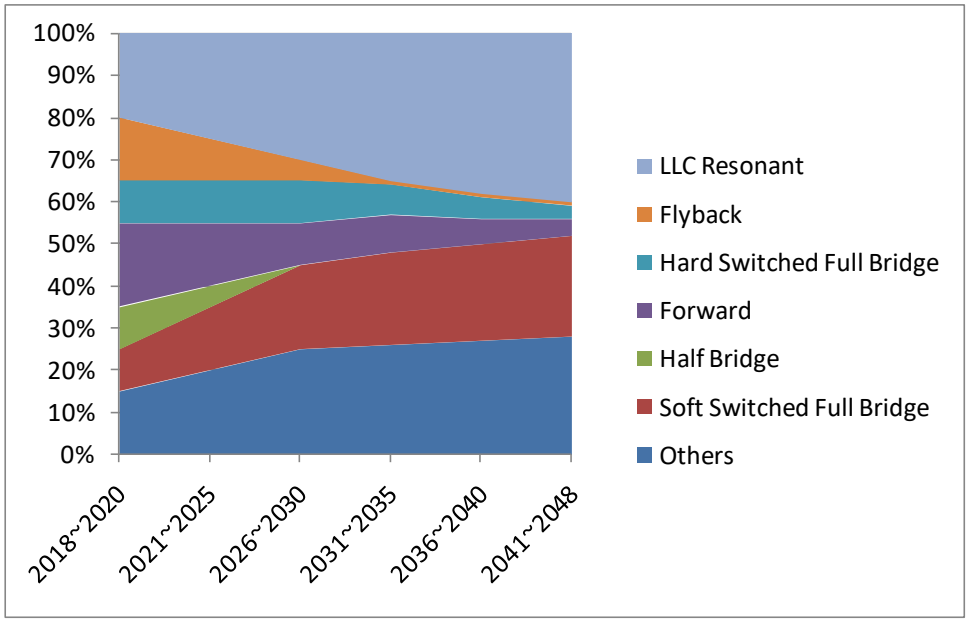


Fig. 2.5 The trend of topology in DC-DC converter

- Application Trend of Transformer (as shown in Fig.2.6)
  - As the power density is increased and the size of the module is limited, the application of planer transformer will become popular.
  - Similarly, the matrix transformer will become more widespread due to the limited module size and dispersed hot spot.
  - The application of discrete transformers will be gradually reduced, and the novel transformer under R&D will be applied in next 30 years.
- Barrier and Challenge
  - The major challenge is to reduce the loss of transformer core under high frequency and improve the transformer wire wrapping density.
- Potential Solution
  - The development and application of new core materials is a potential

solution to reduce transformer core losses at high frequency. The development of new core structures is a potential solution to improve transformer wire wrapping density.

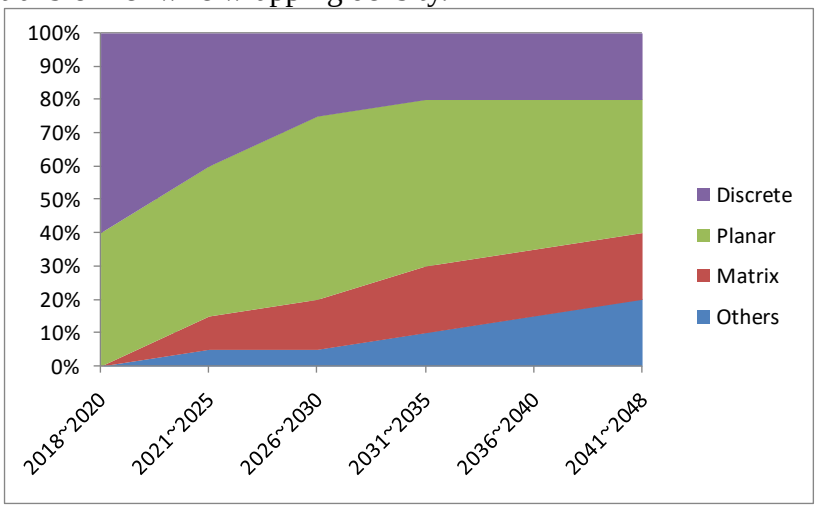


Fig.2.6 The application trend of transformer in DC-DC converter

- Trend of Conversion Efficiency (as shown in Fig. 2.7)
  - For communications modules, for example, the power density is gradually increasing. In order to meet the heat dissipation requirements, the module conversion efficiency should be increased, which is one of the main reasons for the application of the Wide Bandgap semiconductor. In general, the module with higher output voltage have higher conversion efficiency than that with lower output voltage, but conversion efficiency is approaching to the limit due to the losses of the magnetic cores, power devices, auxiliary power supply, and cost consideration (unless the material, topology, packaging technology have a great breakthrough).
- Barrier and Challenge
  - In order to improve the conversion efficiency of the module, high requirements are placed on the electrical design and the thermal design of the module.
- Potential solution
  - New topology, new packaging, the use of high-efficiency Wide Bandgap semiconductor and magnetic core can effectively improve the overall conversion efficiency of the module.

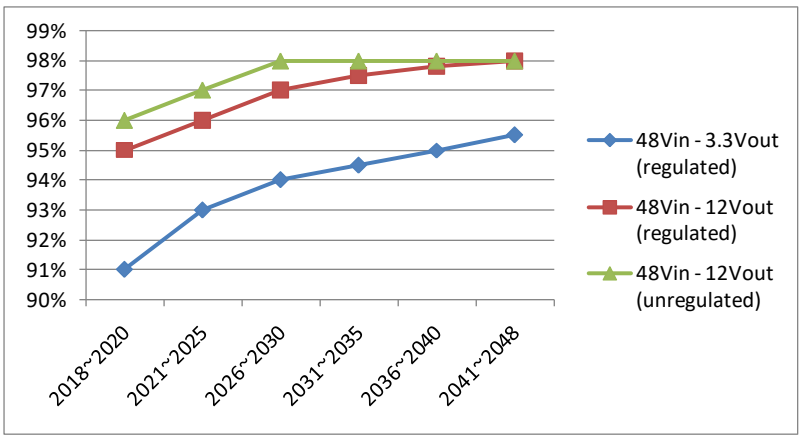


Fig. 2.7 The trend of conversion efficiency of DC-DC converter

■ **MOSFET Module**

➢ Trend of Topology Development (as shown in Fig. 2.8)

- In view of the inverter in motor-control developing towards the direction of high power and high efficiency, the power module packaging technology should exploit the advantage of SiC devices, which is the high power density, high working temperature and high working frequency. However, the high power density and high working frequency will result in switching loss and heat generation, those affect the performance and reliability of power module. Therefore, on the one hand, the current topology should be optimized to reduce the switching loss; on the other hand, new topology should be developed for SiC high power and high frequency application. The cost is also one of the major factors for automotive applications.
- It is believed that, the next generation automotive motor-control inverter module comprises of 3-level three-phase full bridge topology and 3-level phase-leg topology, etc. Due to the cost issue, soft switch three-phase full bridge SiC power module may not be used in vehicle motor driving inverter. At present, 2-level single phase half bridge topology and 2-level three phase half bridge topology are the two mainstream topological design. However, the development of SiC-MOSFET will become mature and the cost will gradually go down, 3-level three phase half bridge topology and 3-level single phase half bridge topology will be widely used and have great potential market share.

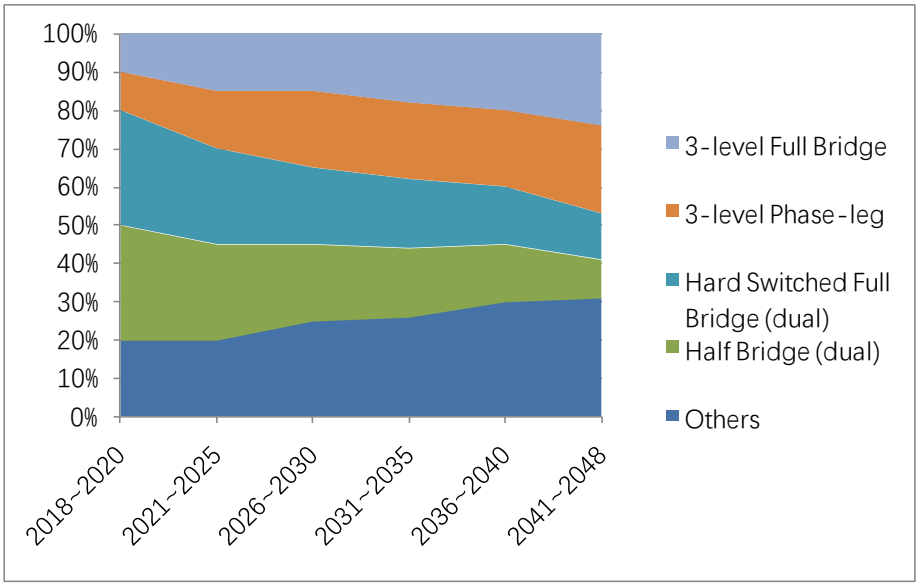


Fig. 2.8 The topology development trend of SiC-MOSFET in inverter for motor driving application

➢ Trend of Conversion Efficiency (as shown in Fig. 2.9)

- In view of the inverter for motor driving developing towards the direction of high power and high efficiency, the key packaging of SiC power module will focus on high frequency performance of SiC devices, so as to improve the working efficiency of the module. On the one hand, it is energy saving and environmental friendly, on the other hand, the heat loss of the chip can be greatly reduced as well as the cost of thermal

management of SiC module and system. To continuously improve the working efficiency of SiC module, the updated chip layout design, electrical topology design and new packaging method should be developed, so that the high frequency and high efficiency application can be achieved. For example, it is reported that, since SiC device has the capability to improve the efficiency of energy utilization, the switching loss of SiC power module is 85% lower than that of Si-based IGBT module.

- 650V, 900V and 1200V are the main voltage levels for inverter in motor driving application with the various current levels from tens ampere to hundreds ampere. The conversion efficiency is different for different voltage levels. There is big difference of conduction loss and junction temperature for different output current, therefore the conversion efficiency would be changed with the change of output current. Herein the conversion efficiency is that when the module is under full loading.
- In the short term, the efficiency of 650V SiC module will be lower comparing to 900V and 1200V SiC module, which is predicted to be around 90%. With the development of device and packaging technology, the final efficiency can reach to ~95.5%, but is still lower than 900V and 1200V SiC module at that time. The highest efficiency of 1200V SiC module targets to be reached to ~99%.

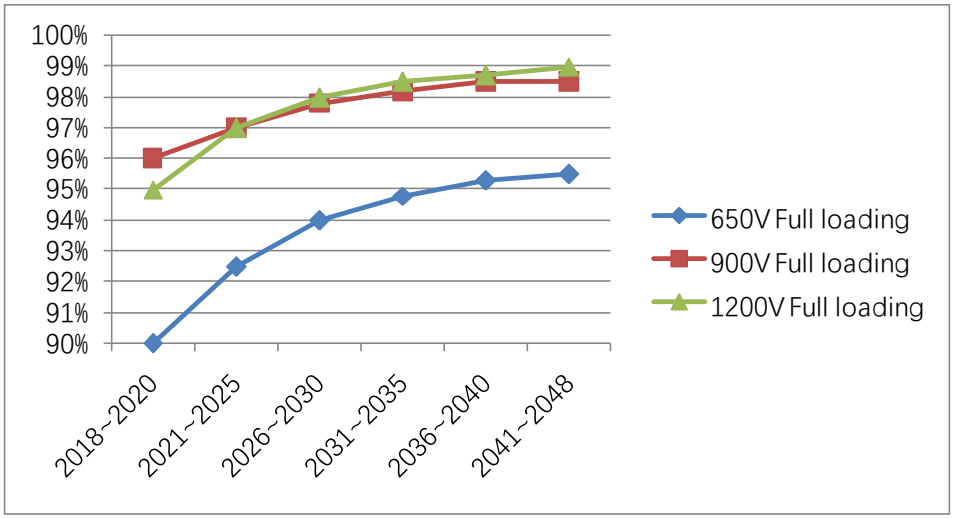


Fig.2.9 The conversion efficiency trend of SiC-MOSFET in inverter for motor driving application

2.4.3 Power and Heat Dissipation

■ **DC-DC Converter**

➢ Trend of Power Density (as shown in Fig. 2.10)

- With the increasing of the integration density of the end system, the industry's requirement to the power density of power module is undoubtedly higher and higher. In the future 5 years, the estimated power density of key products will be ~30W/cm3, and the power density will increase accordingly in an approximate linear way. It is predicted that, the

increase rate of power density will be somehow high in the next 10 years (due to the large-scale popularization and application of Wide Bandgap semiconductor devices), but the power density increase rate will slow down in the next 20 to 30 years, mainly due to the limitation of materials, high temperature and high current.

- Barrier and Challenge
  - Under the limited module dimension, the module should withstand higher current and power, which brings significant challenge to the electrical design, thermal design and packaging design.
- Potential Solution:
  - Fully-molded packaging (or more advanced packaging method) and better thermal design will be the potential solution to break through the limitation of power density.

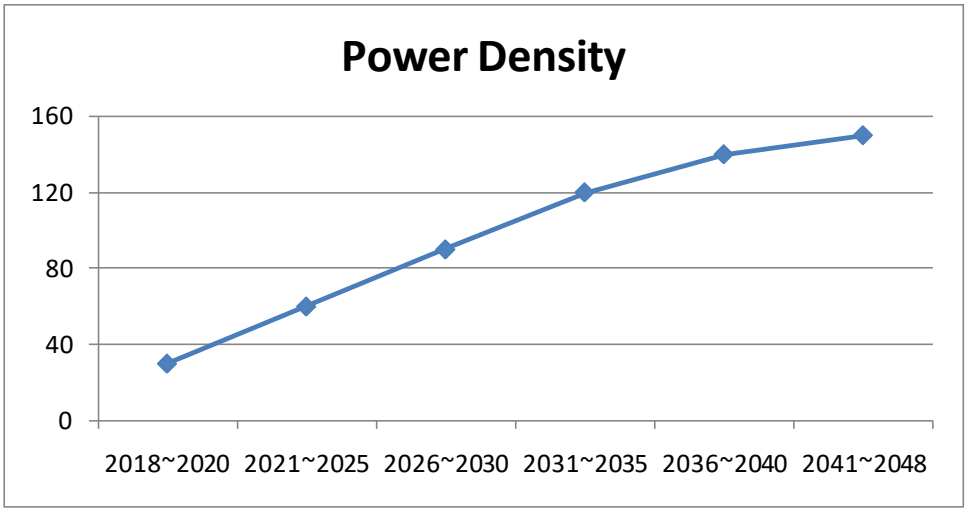


Fig. 2.10 The trend of power density of DC-DC converter (W/cm^3)

■ **MOSFET Module**

- Trend of Power Density (as shown in Fig. 2.11)
  - The power loss of SiC device is ~50% as of Si device, the heat generation of SiC is ~50% as of Si device, and SiC devices has superior high temperature stability. Therefore, the heat dissipation of SiC device is easier under the same power level. The size of heat sink can be reduced, as well as the size and weight of converter can be significantly reduced.
  - Given that the typical application requirement of automotive motor control converter is high efficiency, miniaturization and low cost, new packaging technology (especially high density and miniaturized packaging type) should be developed for automotive motor control SiC converter. The current major problem lies in that conventional electric topological design, layout design, thermal management design and structure design which cannot fully utilize the high frequency and high temperature working characterization of SiC device.
  - The power density of conventional packaged SiC module is above $5\sim10W/cm^3$, which is limited by wire bonding technology and solder alloy interconnection technology. Currently, those are bottlenecks occuring in the overall power density and operating frequency of the module. With the new developed technology such as double-side cooling techniques, planar

packaging and low-temperature nano-silver sintering, the power density of SiC module can be enhanced in future 10~20 years. Furthermore, the SiC chips with higher power density, higher current and higher voltage will launch to market, then the power density of SiC module can be further enhanced with the innovation of 3D packaging, high withstand voltage substrate material and high through-flow substrate material. In the future, the power density can reach to 150W/cm^3 in next 20~30 years, or the maximum power density even reach to 150~180W/cm3.

- In summary, the power density of SiC module will increase dramatically, partially due to the improved capability of heat dissipation. The high temperature working features and packaging as well as the planar packaged SiC module, makes the double-side cooling possible. Furthermore, micro-channel heat dissipation design & manufacturing, micro channel substrate, integrative substrate & heat sink will be created and developed, and becomes the major cooling techniques for high power density SiC module.

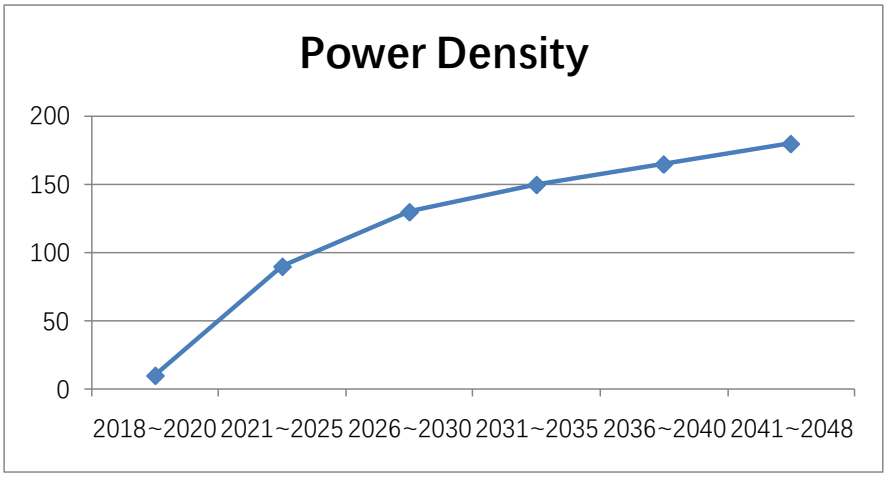


Fig. 2.11 The power density trend of SiC-MOSFET in inverter for motor driving aplication(W/cm^3)

2.4.4 Materials and Process

■ **DC-DC Converter**

➢ Application Trend of Power Device (as shown in Fig. 2.12)

- With the wide application of Wide Bandgap semiconductor, it is believed that the use of Si-based MOSFET will be reduced in the next 30 years. Currently, there are more GaN FET devices used in high-end DC-DC converter, while more SiC MOSFET will be used gradually in various fields and conditions. SiC MOSFET is mainly used in high voltage and high current module, while GaN FET is mainly used in high frequency module. They will also be applied when the development of other Wide Bandgap semiconductors become mature (e.g., Al_2O_3, AlN, Diamond, etc.).

➢ Barrier and Challenge

- The major challenge lies in whether packaging type and structure can exploit the advantage of Wide Bandgap semiconductor devices. The 2nd major challenge is whether the materials can withstand the high current and high temperature in the application of Wide Bandgap semiconductor.

➢ Potential Solution

- The development of new packaging type and application of new packaging materials are needed.

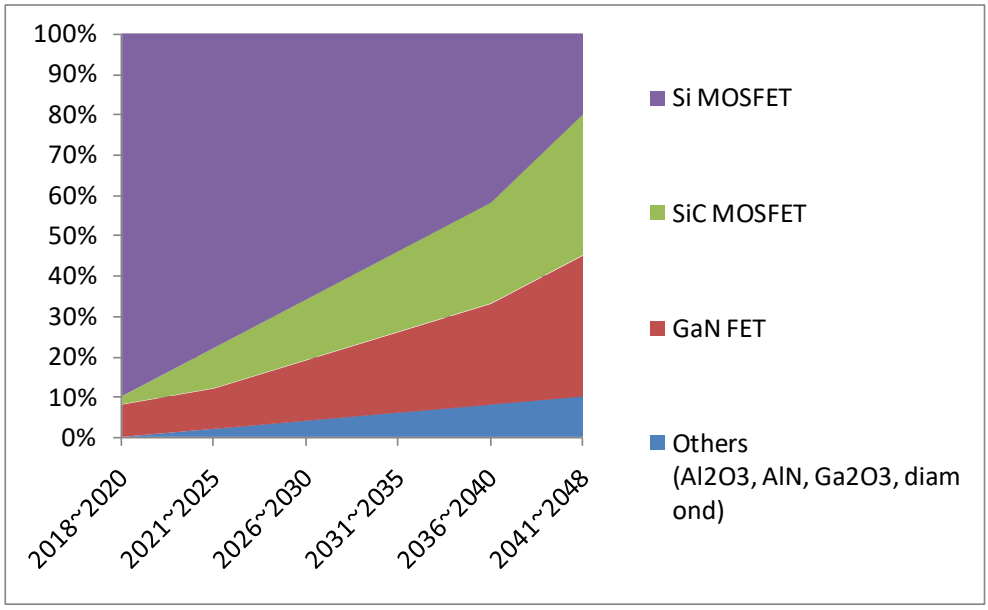


Fig. 2.12 The application trend of power device in DC-DC converter

➢ Application Trend of Substrate (as shown in Fig. 2.13)

- In the next 30 years, the substrate materials for power module can be expected to be dominated by organic materials. Since focusing on increasing power density, current and voltage, the usage of organic substrate will decrease. In return, the usage of insulated metal substrate (IMS) will increase, and share similar usage with organic substrate in next 20~30 years. Meanwhile, the application of ceramic substrate and other materials will be more common.

➢ Barrier and Challenge

- The major challenge for substrate applications is to satisfy the requirement of high power density, high temperature resistance and high heat conduction followed by heat generation as well as the cost reduction. By integrating the substrate with the heat sink and the passive components, further reduction in the size of the system will be a major trend that will also lead to a challenge in process control for new substrate production.

➢ Potential Solution

- The development of new substrate materials and new manufacturing process for substrate are needed.

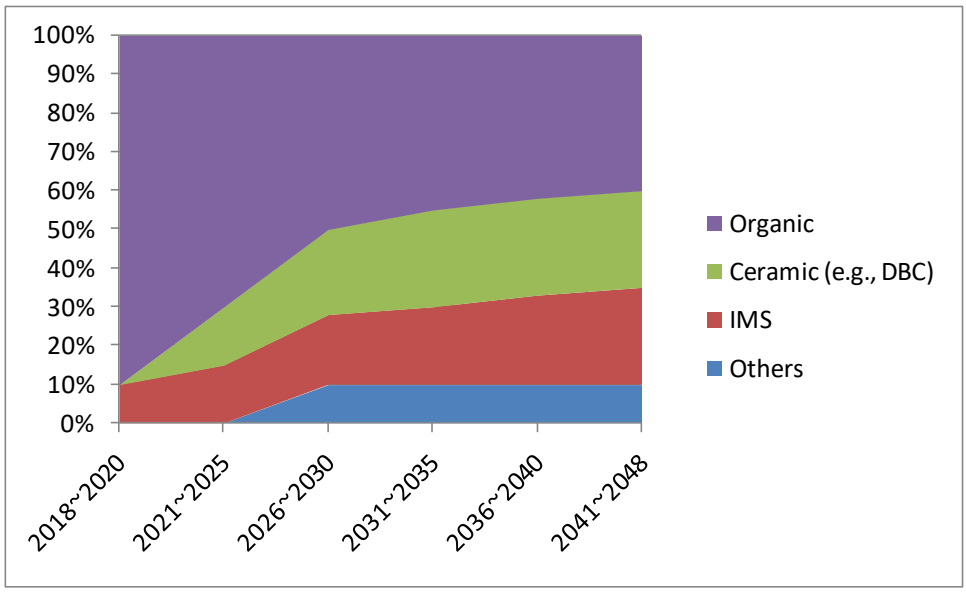


Fig. 2.13 Application trend of substrate of DC-DC converter

- Application Trend of Packaging and Integration Process (as shown in Fig. 2.14)
  - With the increase of integration requirements, the concept of 3D packaging in microelectronics will be applied to power module packaging, and gradually transferred from the 2D packaging to 3D packaging. Currently, two-layer stacked packaging is adopted in high density power module packaging, and stacked packaging with more layers will be expected in the next 20-30 years.
  - In order to satisfy the requirement of high power and heat dissipation, the monopoly status of wire bonding will be replaced by soldering, sintering, and compression etc. Therefore, the vacuum reflow soldering will be more common, since it can effectively reduce the appearance of voids.
  - In order to improve the reliability and level of withstand voltage, underfill process is applied to the bottom of the power device. The gap on the bottom side will become smaller with the increase of integration.
  - In order to increase the throughput and reduce the manufacturing cost, the packaging of power module gradually evolves to board level packaging, and the size of board level packaging is gradually increasing (similar to the increasing wafer size in microelectronics manufacturing).
- Barrier and Challenge
  - In order to be compatible with high power density, the requirement of high temperature resistance, high heat induction plastic molding materials, underfill material and thermal interface materials is much higher.
  - The quality control of the surface mount of the smaller components, the process for the finer L/S interconnects, the direct packaging process for bare die, new process of 3D packaging for power module have to be developed.
- Potential Solution
  - Communication with equipment suppliers to jointly develop the new process for Wide Bandgap semiconductor is needed.

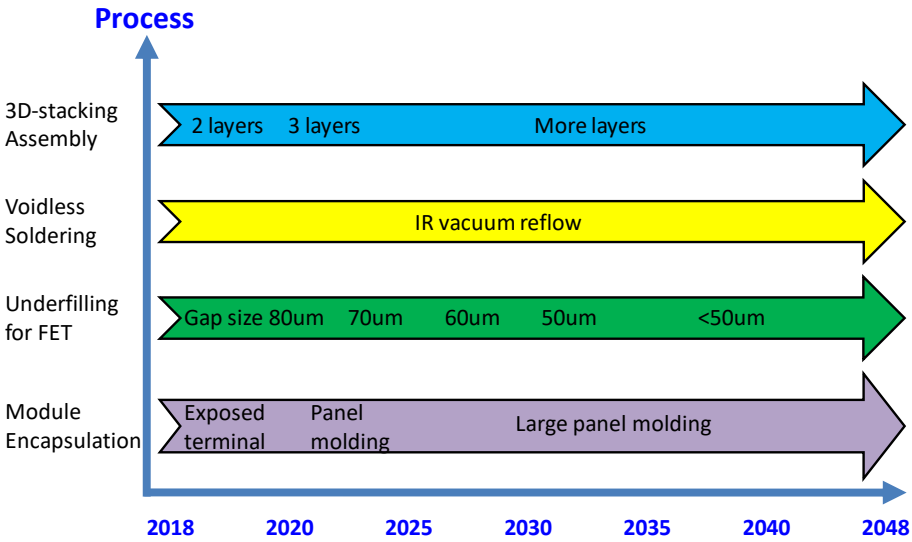


Fig. 2.14 The application trend of packaging and integration process for DC-DC converter

■ **MOSFET Module**

➢ Application Trend of Power Device (as shown in Fig. 2.15)

- For device materials, two Wide Bandgap semiconductor materials SiC and GaN are mainly involved currently. The applications of these two kinds of materials are different. Based on the difference of their own characteristics, GaN device is mostly used in applications of 600-900V, while SiC device is mostly used in applications above 900V.
- It should be pointed out that, GaN also has superior property similar as SiC. However, most of GaN is fabricated through heterogeneous epitaxy on sapphire, Si or SiC substrate, due to the high cost and limitation of equipment of homogeneous GaN substrate. The heat conduction of sapphire substrate is poorer than that of SiC, while the cost is higher, which causes the limitation of the application of GaN materials on power devices. Recently, with the continuously improvement on epitaxy technology, the GaN-on-Si process develops well, and GaN power device for Si substrate develops rapidly. Meanwhile, the homogeneous GaN substrate process improves a lot, therefore GaN power device for GaN substrate also develops. Therefore, in the future, the GaN materials for medium to high voltage power device and even diamond wide band gap device will emerge, and be applied to automotive motor control inverter.

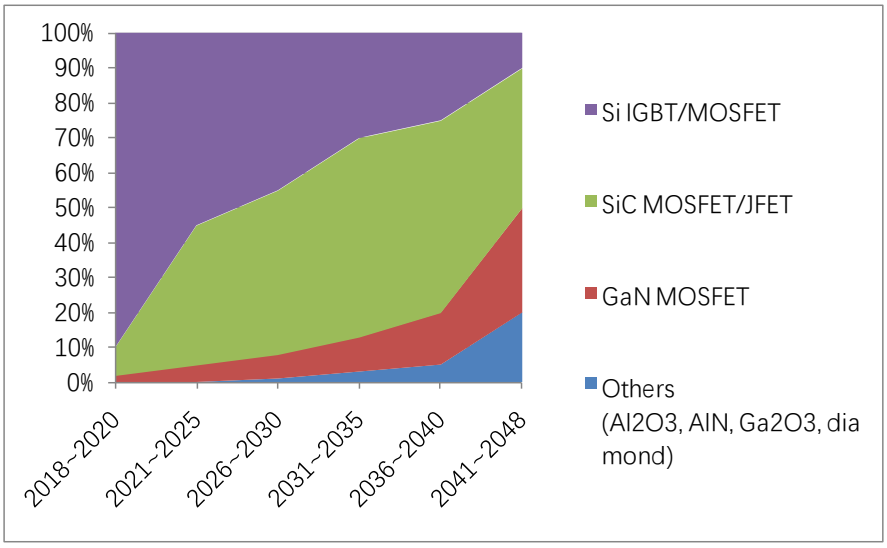


Fig. 2.15 The material of power device in inverter for motor driving application

➢ Application Trend of Substrate (as shown in Fig. 2.16)

- For packaging materials especially substrate materials, the novel substrate materials should require higher thermal reliability, higher insulating strength and cost controllable to fulfill the working conditions under higher working temperature, voltage and current of SiC module. The substrate serves primarily as a support for chips, heat sink, protection, insulation, and interconnection with the external circuitry in the package, so it should have good electrical isolation and heat dissipation. The packaging substrate should have better high temperature reliability since the working temperature of Wide Bandgap semiconductor is high. The next generation high reliability substrate for SiC module packaging includes organic substrate, ceramic substrate, insulated metal substrate, etc.
- In the application of EV, ceramic substrate is the major substrate solution. The substrate normally comprises of insulated layer and plated metal. The most common insulated layer material is Al_2O_3, and in the future, the usage of AlN and Si_3N_4 will be higher since they have higher conductivity. It must be pointed out, although the DBC (Direct Bonded Copper) / aluminum substrate is most commonly used, its low resistance to high and low temperature impact and its bonding strength are not satisfied. Therefore, in the future, AMB (Active Metal Brazing) based DBC / aluminum substrate will become a new trend. IMS and ceramic substrate have the advantage of cost, while IMS has good insulation withstand voltage performance and cost controllable, it will be a trend in the future.
- Furthermore, it is required to pay more attention to the multi-layer DBC and ceramic substrate with integrated heat sink which can withstand high working voltage and high switching frequency, and the multi-layer DBC has the following features: (1) To lower down the electric field intensity and avoid local discharge breakdown; (2) To improve heat dissipation performance and reduce the junction temperature; (3) To reduce the parasitic inductance and reduce the common mode current to satisfy the high frequency switching requirement. Even though the process is complicated and the cost is high, it has the possibility to be key substrate

material of SiC module.

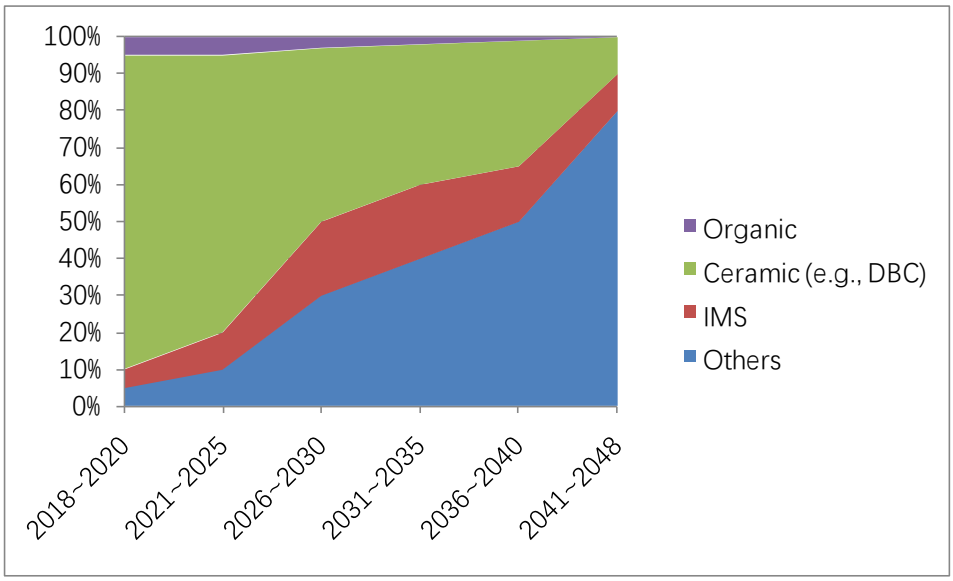


Fig. 2.16 The application trend of substrate in inverter for motor driving application

- Application Trend of Interconnect
  - For the interconnect materials, the high working temperature reliability of SiC chip will be the major focus. The melting point of conventional solder alloy is normally below 400 °C, which explains its working temperature cannot exceed 200 °C otherwise, high temperature fatigue aging will occur and severely affect the reliability of module. Therefore, the low temperature sintering silver materials and transient liquid phase alloy interconnect materials will be widely used. It must be pointed out that, the melting point of intermetallic compound (IMC) after the interconnects formed by transient liquid phase alloy interconnect material is about 600 °C, which is still lower than the melting point of sintering silver at 960 °C. Besides, IMC after the interconnects formed by transient liquid phase alloy interconnect material will have brittle change, which will affect the reliability of the module. Therefore, transient liquid phase alloy interconnect material will encounter challenges in the development of SiC device.
  - In view of the applications of new packaging modules such as planar packaged SiC module, double-sided cooling planar SiC module and double-sided stacking SiC module, new encapsulate materials are required to satisfy the requirement of high density packaging. The molding and encapsulate materials for SiC module should fulfill high temperature resistance, high heat conduction, good liquid filling, tunable coefficient of thermal expansion, excellent gas tightness. The encapsulation materials for EV applications should focus on high temperature resistance, low modulus and good bonding strength in the substrate. The current organic encapsulate and molding materials cannot meet the packaging requirement as >400°C, vacuum ceramic/metal packaging will be a better solution.

2.4.5 Reliability

■ **DC-DC Converter**

➢ Lifetime Trend (as shown in Fig. 2.17)

- Currently, power module is commonly applied in consumer electronics and telecommunication. If the usage of Wide Bandgap semiconductor increases and the power density improves, the power module applied for industrial, EV, military, aerospace will also gradually increase. Thus, the lifetime requirement for power module will be higher.

➢ Barrier and Challenge

- New failure and reliability mechanisms need to be further studied as the new materials, new devices and new processes are involved.
- High power, high current and high power loss bring multiple and complicated failure mechanisms.
- The lowering cost and shorter commercialization time bring great challenge to the study of failure mechanism.

➢ Potential Solution

- Design for reliability by using numerical simulation and analysis tools is needed at the beginning phase of product design.

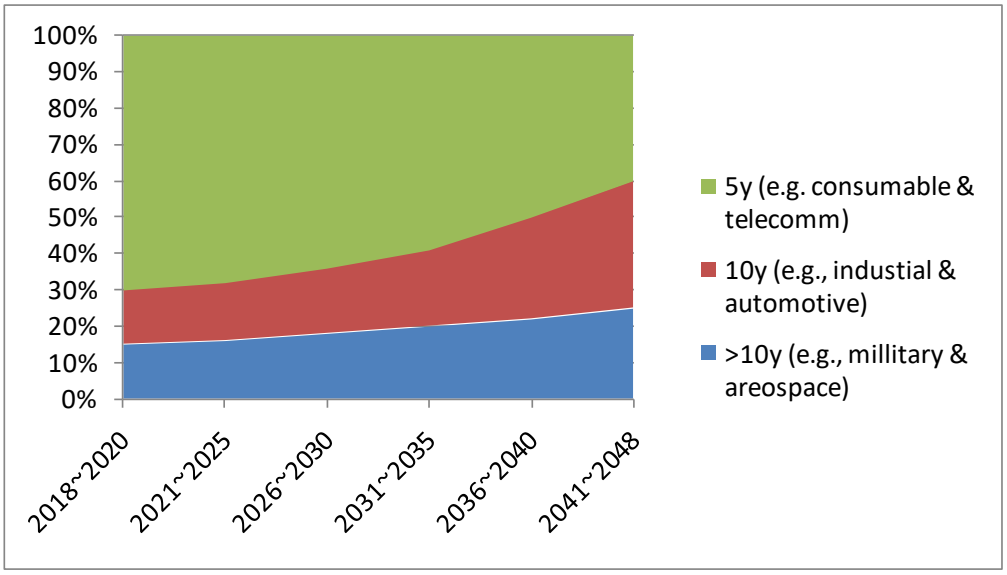


Fig. 2.17 The lifetime trend of DC-DC converter

■ **MOSFET Module**

➢ Reliability Trend (as shown in Fig. 2.18)

- The reliability of the SiC module is the ultimate and key purpose for module packaging. Since the power density, working temperature and working frequency of SiC module will gradually increase in the future, it is a must to develop comprehensive multi-physics solution for SiC power module design, and thereby solving the electrical, thermal, radiation and thermal mechanical problems in low voltage (e.g., 600~3300V), medium voltage (e.g., 3.3~10kV), and high voltage (e.g., 10~24kV) for SiC applications. Otherwise, the reliability of SiC power module（e.g., high and low temperature thermal shock, thermal cycling, high temperature and

humidity test, the aging test under harsh environment, etc) will be affected and cannot function well.

- In the future, the power devices are mainly used in industrial electronics, EV, aerospace and military applications. The reliability requirements will vary depending on different applications. In industrial electronics, the lifetime of SiC module is designed to be ~10 years. In EV and high-speed traction, the lifetime is expected to be ~15 years. In aerospace and military application, the lifetime is required to be >15 years. For example, the lifetime of power devices in Mars rover is >30 years.
- Considering that the performance, power density and reliability requirements of industrial electronics is far below than that of EV, aerospace and other high-end applications, the needs for industry-used SiC module are not remarkable and Si-based IGBT/MOSFET power module is more common, except for some special conditions. It is noteworthy that, the usage of SiC module in EV applications (except for high power motor driving) such as in EV charger and motor-mounted power source will be increased in the future.
- Motor drive for EV will be the main battlefield for the future SiC modules in the civilian market. It is because the unit output power of EV power source module is more than dozens of kilowatts, and even expected to be hundreds of kilowats. This causes the p-n junction temperature arising dramatically due to the power loss heat generated by power electronics devices, which will easily exceed the specified working temperature limitation (the temperature limitation of Si-based device is 125~150^{o}C). Therefore, in order to effectively control the operating temperature of power electronics devices, and to ensure the conversion efficiency and reliability, the motor driving in EV needs to design a large-capacity cooling system, which is the key factor affecting the cost and endurance of hybrid vehicles. Due to the high temperature operating characterization and high temperature packaging solution, the cost of thermal management of control system can be effectively reduced. Moreover, the SiC module with high-frequency capability enables the controller to be significantly reduced in size and weight with a high-density package design. The abovementioned advantages for the development of future EV is essential. Therefore, to ensure the reliability of SiC module and improve the service life, the high temperature resistant packaging materials should be generously developed. The high packaging density structure design and low stress packaging integration process should be strongly promoted.
- It must be pointed out that, the lifetime requirement for aerospace SiC module needs to be very high, and the operation condition is very complicated, thus the requirement for packaging material, packaging design and process is high. The plastic molded packaging solution cannot meet the strict requirement, so the fully-metal packaging high-density SiC module should be focused for the aerospace application. The reliable working temperature of future packaging material would be in the range of -100~300^{o}C. The metal packaging shield can be manufactured by 3D printing integrative shield in order to enhance the sealing. The packaging material should also have good capability of radiation resistant.

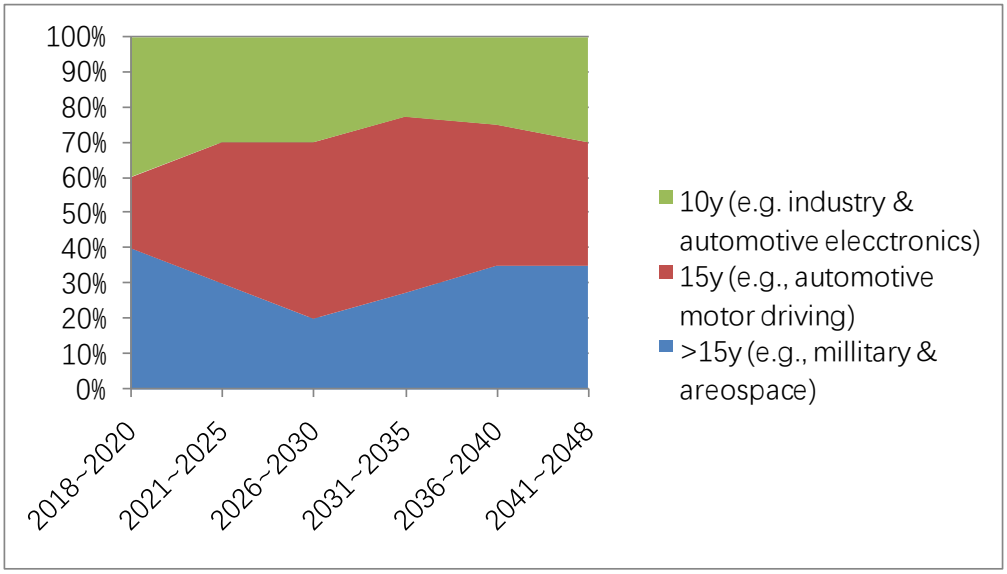


Fig. 2.18 The lifetime trend of power module in inverter

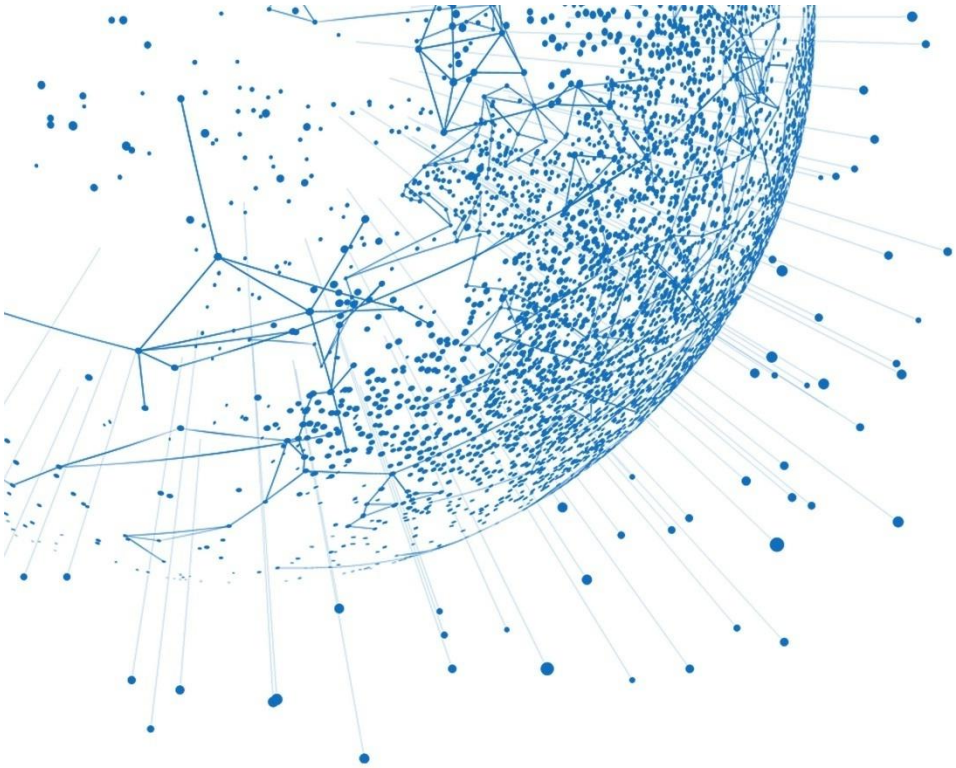
2.5 Summary

With the popularization of Wide Bandgap semiconductor, the factors such as market, cost, integration density, power density and the requirements of power, current/voltage, heat dissipation, frequency, conversion efficiency, extreme conditions, lifetime have big change. With the impact and promotion of these factors, it is believed in the future 30 years the Wide Bandgap semiconductor based packaging technology and module type will have following changes:

- Structure and Dimension: the packaging module will become high integration, miniaturization, integrative packaging.
- Electrical Performance: the application of LLC resonance and phase-shift full-bridge soft switch topology will be widely used in DC-DC converter. 3-level three phase full bridge topology and 3-level single phase half bridge topology will be widely used in MOSFET in inverter for motor driving application. More advanced topologies will be developed and used in next 30 years.
- Power and Heat Dissipation: with the continuous development of heat dissipation technology, the power density of module will increase, and is expected to reach 150~180W/cm^3 in next 30 years (unless materials, structure, process, application have great breakthrough, it is near to the limitation).
- Materials and Processes: as for the power module, it is believed that the applications of Si-based device will decrease, while the applications of Wide Bandgap semiconductor will increase, especially SiC device and GaN device. As for substrate materials, the organic substrate for DC-DC converter is still dominant in next 30 years, but the percentage will gradually decrease. The insulated metal substrate and ceramic substrate are suitable for high power, high current, high voltage applications. The packaging type will transform from 2D packaging to 3D packaging, and the 3D packaging process will

improve a lot.

- Reliability: due to the outstanding performance of Wide Bandgap semiconductor, the applications of power module in industrial, EV, military and aerospace will increase, thus the reliability requirement will be higher.



SiC Applications

In recent years, “energy conservation and emission reduction” and “development of green energy” have become the basic national strategies for long-term development in China. Driving by the development of green energy industry, the rapid development of power electronics technology has become one of the important supporting technologies for building a conservation-oriented society, promoting national economic development and implementing the innovation-driven development strategy.

SiC devices have begun to replace Si devices, and the replacement speed is accelerating. Based on the present status of SiC devices, we are trying to predict the development trend and overall application trend of the SiC devices. Finally we focus on the application opportunities of SiC devices in power grid, electric traction, uninterrupted power supply, electric vehicles, household appliances and consumer electronics.

3.1 Status of SiC devices

As of June 2018, there are four SiC products, including SiC diodes, SiC MOSFETs, full SiC modules consisting of SiC diodes and SiC MOSFETs, and hybrid modules consisting of SiC diodes and Si IGBTs.

Take the Wolfspeed Company of the United States as an example to illustrate the general level of SiC diode and SiC MOSFET products.

- SiC MOSFET discrete products: 900 V/ (11.5-36 A), 1000 V/ (22-35 A), 1200 V/ (10-90 A) and 1700 V/ (5.3-72 A);
- SiC MOSFET die products: 900 V/ (36-196 A), 1000 V/ 36 A, 1200 V / (19-98 A), 1700 V/ (40-72 A);
- SiC diode discrete products: 600 V/ (1-20 A), 650 V (2-50 A), 1200 V/ (2-40 A), 1700 V/ (10-25 A);
- SiC diode die products: 600 V/ (1-10 A), 650 V/ (4-50 A), 1200 V/ (2-50 A), 1700 V/ (10-50 A);
- Full SiC module products: 1200 V/ (20-325 A), 1700 V/ 225 A (half-bridge).

The hybrid module is illustrated by taking Mitsubishi Electric of Japan as an example: 600 V/ (20-200 A), 1200 V/ (100-600 A), 1700 V/ 1200 A.

3.2 Development trends of SiC devices

In general, power electronic devices are developing toward the direction of higher voltage, higher current density, lower conduction voltage drop, and higher switching frequency. The overall development trends of SiC products:

- The voltage and current of SiC products will be further improved;
- The switching frequency will be further increased;
- The cost of SiC products will be reduced continuously. Devices such as SiC diodes and SiC MOSFETs are expected to drop by more than 10% a year in

prices, and have begun to replace the Si devices gradually;

- The reliability of SiC products will be further improved;
- The type of SiC products will be rich and diverse. Products such as SiC IGBT and SiC thyristors will be developed.
- There will be more integrated driving SiC products, such as driver and chip integration, light triggered and integrated short-circuit protection.
- There will be more customized SiC products, such as photovoltaic modules etc.

3.3 The overall technology roadmap of SiC device applications

3.3.1 Competitive analysis of SiC devices and Si devices

The basic development trend of power electronic device design is based on reducing switching losses, and to increase the switching frequency, reduce the size of magnetic components, reduce the volume and size of radiator, hence enhance the power density.

The advantages of SiC devices include at least the following:

- When commutation by the same SBD, the turn-on loss of SiC devices is significantly less than that of Si devices with a reduction of 25~50%.
- The turn-off loss of SiC devices is about 5-10 times lower than that of Si devices.
- The influence of the temperature on the turn-off loss of SiC devices is much less than that of Si devices.
- The conduction loss below the rated current of SiC devices is usually lower than that of Si devices.
- Theoretically, the highest operating junction temperature of SiC devices (existing 200 °C products) is higher than that of Si devices.
- SiC diode does not have forward recovery voltage or reverse recovery current.
- The gate drive charge of the SiC devices is less than that of the Si devices.
- As a unipolar device, SiC MOSFET can greatly increase the blocking voltage of the device under the premise of ensuring low on voltage drop. The blocking voltage of SiC MOSFET has reached 10KV.

The disadvantages of SiC devices include at least the following:

- The gate threshold voltage of SiC devices is usually lower than that of Si devices, which is easily triggered by the influence of dv/dt. At the same time, there are some reliability defects such as gate threshold voltage drift.
- The duration of SiC devices to withstand short-circuit current is less than that of Si devices.

3.3.2 Driving force

Current SiC products have a maximum voltage of only 1700 V, which can be

applied only in situations where the voltage is low and the current is small. The current of hybrid SiC modules can be more than 1000 A. Compared with Si modules at the same current and voltage level, the performance advantage of hybrid SiC modules is obvious. Besides, their cost and reliability is more acceptable to the users than full SiC module products. Accordingly, there is a large application market in the field where high energy conversion efficiency is required. With the development of SiC products toward high voltage and high capacity, there will be more application fields and amounts of SiC products. However, for small capacity converters with applied voltage of 600 V and below, in addition to facing the strong competition with existing Si MOSFETS, SiC products may also be impacted by GaN devices.

SiC product applications include at least power grid, power traction, power supply, electric vehicle, household appliance, medical equipment, and consumer electronic products, etc.

SiC products can be tested or applied at least in switching power supply, elevator control system, track traction inverter, EV/ HEV motor drive, air conditioning, photovoltaic, electric vehicle charging pile, large construction machinery, solid state circuit breakers, induction heating, power electronic transformer, etc.

From the technical point, there are several driving forces to replace Si products with SiC products. Of course, for a specific product, the technical driving forces may be a combination of following items.

(1) Lower losses, including the on-state loss and the switching loss. Taking LCC-HVDC at ± 800 kV and rated current of 5 kA as an example, it is estimated that the power loss can be reduced by about 47% through using SiC products. As another example, for the same capacity converter, using high voltage SiC products can reduce the current of the converter, thereby improving the conversion efficiency of the converter.

(2) Reduce the complexity of the device. Replacing relatively low-voltage Si products with high-voltage SiC products to reduce the amounts of power electronics or/ and modules, and hence to reduce the complexity and improve the reliability of the device;

(3) Decrease the levels of power conversion. High-voltage SiC devices (SiC devices with a voltage of 10 kV or more) can reduce the frequency of power conversion, such as the saving of the step-down transformer and so on;

(4) Increase the switching frequency. For example, motor drive, etc., can provide output voltages with a higher frequency;

(5) Improve the applicability. By increasing the switching frequency, reducing the volume of reactors, capacitors and transformers, and reducing the weight, the applicability of the device can be improved on occasions like ships and vehicles;

(6) Reduce the requirement for system heat dissipation. Due to the low loss caused by SiC, the system efficiency is improved, which reduces the difficulty and the cost of the system cooling design. As another example, in the power grid reconstruction, the conventional transformer is replaced by the power electronic transformer, and the SiC is used to solve the problem of

site limitation in the transformation.

(7) The need of special operating environment. For example, Si products are not applicable when the ambient temperature is relatively high.

3.3.3 Differentiated development

In 2017, the market share of SiC devices is about $302 million, and it is expected to reach about $1.4 billion by 2023. Electric vehicles, PV and high efficiency power supply will be the focus of SiC devices. The application of SiC presents the following three aspects of differentiated development:

- SiC provides naked products. Unless the main customers, usually do not provide bare Si based devices.
  1) SiC has no ideal encapsulation.
  2) It is convenient to make full use of the advantages of SiC devices, but the application difficulty is increased.
- SiC diode products. It is relatively easy to use, and the price gap between Si-based products is smaller. There are lots of commercial applications in the power supply of Bitcoin ant diggers, and there are many applications in high-efficiency (data center) power supply, PV, charging pile.
- SiC MOSFET products. The application is relatively difficult (such as the high DV / dt problem caused by too fast switching), and the price gap between Si-based products is larger. They have been tried out in PV inverter, charging pile, electric vehicle charging and driving, power electronic transformer and so on.

3.3.4 Common weaknesses

Compared with Si products, SiC products have two common weaknesses:

(1) The price is too high. At this stage (December 2017), the price of international SiC products is 5 to 6 times that of corresponding Si products, and the price of domestic SiC products is higher, some of them even reaches 10 times. The price of SiC products depends mainly on the wafer. If the price of SiC MOSFET products falls to 2 times of the corresponding Si products, SiC products will be more competitive in the market. Products with strong demands for volume or weight and costume products or projects are less sensitive to the price of SiC products.

(2) The reliability has not been verified by a sufficient number of applications. Compared with Si IGBT, the robustness of SiC MOSFET devices is slightly worse after all. Reliability data need to be verified, especially the lifetime of metal oxide layer, the reliability of bulk diodes and the threshold voltage drift. Currently, the SiC MOSFET products are tested according to the corresponding test items and methods of Si products, and no specific test items and methods have been designed for the features of SiC MOSFET products. Reliability standards and tests for SiC are the technical bottlenecks.

Some EV/ HEV manufactures are concerned much about the reliability of SiC products. The whole vehicle needs to be recalled if the SiC products are defective, and the corresponding economic losses will be very large.

3.4 Technical route of SiC devices in power grid application

This part will be illustrated from several representative directions including DC transmission, flexible substations, flexible AC transmission, photovoltaics and solid state switches. The application in wind power can refer to the flexible AC transmission based on full-controlled device related contents.

3.4.1 DC transmission

3.4.1.1 Introduction

DC transmission mainly includes Line-commutated converters – High Voltage Direct Current (LCC-HVDC), Voltage-source converters – High Voltage Direct Current (VSC-HVDC), Hybrid HVDC, DC grid, etc. Among them, Hybrid HVDC and DC grid had not been applied to the engineering project until December 2017. At this stage, all of the LCC-HVDC employs Si thyristors, while all of the VSC-HVDC employs Si IGBTs. LCC-HVDC will be gradually replaced by VSC-HVDC.

In DC transmission, the maximum rated current is 6250 A and the highest rated voltage is 1100 kV. The possibility of DC transmission over 6250 A and 1100 kV is not large.

3.4.1.2 Driving forces

The driving forces of the application of SiC devices (including hybrid SiC devices) in DC transmission are (1), (2), (5) and (6) in section 3.3.2. Due to the relatively low switching frequency of HVDC, reducing losses is mainly to reduce the on-state loss. It should be noted that the reduction of heat dissipation requirements usually results in a reduction in the footprint and volume of the device.

3.4.1.3 Requirements for device

- SiC products: Voltage ≥ 10 kV, current ≥ 1.0 kA;
- Use press pack to ensure the short current failure;
- A low on-state voltage drop is required to improve overall efficiency;
- For the MMC VSC-HVDC, an antiparallel diode is required to withstand large inrush currents.
- Tolerance of rated current is large, long-time, and strong after shutdown.

3.4.1.4 Development forecast

At this stage there is no SiC IGBT related products, hybrid module capacity (1700 V/ 1200 A) is still relatively small. Here we just make a brief forecast.

- The popularization and application of hybrid SiC devices should be earlier than that of pure SiC devices;
- By 2030, 3300-6500 V/ 1500-3000 A series Si IGBT + SiC Diode hybrid devices will be demonstrated in VSC-HVDC applications;
- By 2048, the conversion efficiency of SiC MMC-HVDC is expected to be as

high as 99.8%.

Table 3.1 Development prediction of flexible DC converter valve

	2020	2025	2030	2035	2040	2048
Voltage level (DC)	±50kV	±50 kV	±100 kV	±200 kV	±320 kV	±400 kV/500 kV/800 kV
Capacity MW	50	100	500	1000	2000	5000
Device	MOSFET	IGBT	IGBT	IGBT	IGBT	IGBT
Device parameter	6.5kV/600A	15kV/600A	15kV/1000A	20kV/1000A	20kV/2000A	20kV/2500A
Converter valve efficiency	98	98.5	99	99.5	99.6	99.8

3.4.2 Flexible substations

3.4.2.1 Introduction

Flexible substations/ transformerless intelligent power substations (TIPSs) typically include power electronics such as power electronic substations/ solid state transformers and solid state circuit breakers. Here we focus on power electronic transformers, solid state circuit breakers will be discussed in the section 3.4.5 solid state switches.

The minimum AC voltage of power electronic transformers for power grids should not be less than 10 kV (grid nominal voltage) and the minimum capacity (three phases) should not be less than 315 kVA. The maximum AC voltage is 1000 kV (grid nominal voltage) and the maximum capacity is 10 million kW. It's not likely to happen that the maximum voltage and the maximum capacity of power electronic transformer used in power grids exceed 1100 kV and 10 million kW, respectively.

3.4.2.2 Driving forces

The driving forces of SiC devices in power electronic transformers are (1), (2), (4), (5) and (6) in section 3.3.2.Power electronic transformers are more concerned with efficiency, volume and weight.

3.4.2.3 Requirements for devices

- Voltage ≥ 10 kV;
- Switching frequency ≥ 10 kHz;
- Current ≥ 20 A.
- Tolerance of rated current is large, long-time, and strong after shutdown.

3.4.2.4 Development forecast

There are relatively more researches of application in power electronic transformers.

- In 5 years (up to 2023), the capacity of the three-phase PET prototype should be 315 kVA or more. The conversion efficiency of a three-phase PET prototype with a system nominal voltage input of 10 kV or 6 kV and output of 220 V/ 380 should be able to reach 98.3% or above.
- In 5 years (up to 2023), engineering demonstration application of 35 kV/ 5

MVA full SiC power electronic transformers with 6500 V SiC MOSFETs could be achieved.

- By 2030, 15 kV SiC bipolar devices could be demonstrated to be applied to 500 kV power electronic transformers. SiC power diodes include high-voltage PIN diodes, bipolar transistors (BJTs), insulated gate bipolar transistors (IGBTs), thyristors, GTOs, silicon carbide GCTs, etc.

Table 3.2 Development prediction of power electronic transformer (PET)

	2020	2025	2030	2035	2040	2048
Voltage level (AC)	35kV	35 kV	110 kV	220 kV	330 kV	500 kV
Capacity MVA	50	100	500	1000	2000	5000
Device	MOSFET	IGBT	IGBT	IGBT	IGBT	IGBT
Device parameter kV/A	6.5kV/600	15kV/600	15kV/1000	20kV/1000	20kV/2000	20kV/2500
PET efficiency	98	98.4	98.8	99.1	99.3	99.4

3.4.3 Flexible AC transmission

3.4.3.1 Introduction

According to the controllability of power electronic devices applied, Flexible AC transmission system (FACTS) can be divided into FACTS devices based on half-controlled power electronic devices such as thyrsitor controlled series capacitors (TCSCs) and static VAR compensators (SVCs), and FACTS devices based on full-controlled power electronic devices, such as static synchronous compensators (STATCOMs) and unified power flow controllers (UPFCs) and so on. At this stage, thyristors are used in FACTS devices based on half-controlled power electronics, and Si IGBTs are used in FACTS devices based on full-controlled power electronics. FACTS devices based on full-controlled power electronics will gradually replace FACTS devices based on half-controlled power electronics.

According to the way that the converter is connected to the power grid, it can be divided into series FACTS devices, such as thyristor controlled series compensators (TCSCs), static synchronous series compensators (SSSCs), fault current limiters (FCLs), etc.; parallel FACTS devices, such as static var compensators (SVCs), static synchronous compensators (STATCOMs), controllable shunt reactors (CSRs), etc.; series-parallel FACTS devices, such as unified power flow controllers (UPFCs), convertible static compensators (CSCs), variable frequency transformers (VFTs), etc.

It is unlikely that the rated current in the series part will exceed 6300 A, and the maximum ac voltage in the parallel part is 1000 kV (nominal grid voltage).

3.4.3.2 Driving forces

The driving forces of SiC devices (including hybrid SiC devices) in FACTS are (1), (2), (5) and (6) in section 3.3.2. Due to the relatively low switching frequency of

the FACTS, reducing losses is mainly to reduce the on-state loss. It should be noted that the reduction of heat dissipation requirements usually results in a reduction in the footprint and volume of the device.

3.4.3.3 Requirements for device

- Use press pack package to ensure short circuit failure;
- A low on-state voltage drop is required to improve overall efficiency;
- For the MMC VSC structure, anti-parallel diodes are required to withstand large inrush currents.
- Tolerance of rated current is large, long-time, and strong after shutdown.

3.4.3.4 Development forecast

- The popularization and application of hybrid SiC devices should be earlier than that of pure SiC devices;
- Among FACTS devices based on fully controlled power electronics, STATCOMs are most likely the first to be applied.

Table 3.3 Development prediction of flexible AC transmission system (FACTS)

	2020	2025	2030	2035	2040	2048
Voltage level (AC)	35kV	35 kV	110 kV	220 kV	330 kV	500 kV
Type	APF	STATCOM SSTS	STATCOM SSTS	STATCOM SSTS	STATCOM SSTS	UPFC
Capacity MVA	5	10	50	100	200	500
Device	MOSFET	IGBT	IGBT	IGBT	IGBT	IGBT
Device parameter	6.5kV/600A	15kV/600A	15kV/1000A	20kV/1000A	20kV/2000A	20kV/2500A
Efficiency	97	97.5	98.4	99.1	99.6	99.6

3.4.4 Photovoltaic system

3.4.4.1 Introduction

Photovoltaic inverters mainly include micro inverters mounted on photovoltaic panels, string photovoltaic inverters for roof photovoltaic system, and centralized photovoltaic inverters for photovoltaic substations.

By December 2017, the maximum output power of Enphase's micro inverters is between 240 and 320 W. As to the products of Sungrow Power Supply Co.,Ltd. , the output power of single-phase string photovoltaic inverters is3-8 kW, the output power of three-phase string photovoltaic inverters is 10-80 kW, and the rated output power of the centralized photovoltaic inverter is 500-1500 kW.

Si devices are widely used in current photovoltaic inverters. After more than 40 years of development, the conversion efficiency and power density are close to the theoretical limit. For further improvement, SiC and other wide band gap devices are

the inevitable choice. With hybrid SiC power modules, the conversion efficiency of photovoltaic inverters should be improved to a certain extent. For instance, Mitsubishi Electric introduced a 600 V/ 50 A hybrid SiC H-bridge power module, but this should be a transition in SiC devices replacing Si devices. The length of this transition time depends mainly on the time required to gradually resolve the two common weaknesses in section 3.3.4.

3.4.4.2 Driving force

The driving forces of SiC devices (including hybrid SiC devices) in photovoltaic inverters are (1), (4), (5) and (6) in section 3.3.2. Reducing losses is mainly to reduce the switching loss. High-voltage devices could also be utilized to reduce the number of power electronics, reduce the current value and improve the conversion efficiency of the device.

3.4.4.3 Requirements for devices

- SiC products for string inverters: switching frequency ≥ 50 kHz;
- SiC products for centralized photovoltaic inverter: switching frequency ≥ 10 kHz;
- Low switching loss is required to improve the conversion efficiency of the device;
- The price should be as low as possible because the photovoltaic inverter products are relatively sensitive to it.

3.4.4.4 Development forecast

High efficiency, high power density, high reliability and low cost are the future trends of photovoltaic inverters. SiC products will gradually replace Si products in both string and centralized photovoltaic inverters.

- String photovoltaic inverters: In 5 years (up to 2023), the maximum conversion efficiency of single-phase 3 kW products should be greater than 99.50%, and the weight should be less than 7.5 kg. The maximum conversion efficiency of three-phase 50 kW products should reach 99.50%, and the weight should be less than 33 kg which is better than 1.5 kW/ kg. SiC devices have been used in a small scale, and especially MPPT boost circuit has mass-produced products due to the increase of switching frequency. But the application of inverter side circuit is still in the stage of test or small batch production. It is expected that SiC devices will basically replace the Si devices within 10 years.
- Centralized photovoltaic inverters: SiC hybrid devices are preferred to be applied. Within 5 years (up to 2023), the maximum conversion efficiency of the products with a rated power of 500 kW should be up to 99.20%.

Table 3.4 Development prediction of photovoltaic inverter

	2020	2025	2030	2035	2040	2048
Voltage level (AC)	0.4kV	10 kV	35 kV	110 kV	110 kV	220 kV
Type	Cluster	Centralized	Centralized	Centralized	Centralized	Centralized
Capacity	3-10kW	500-1500	3-5MW	10MW	20MW	50MW

		kW				
Device	MOSFET	MOSFET	IGBT	IGBT	IGBT	IGBT
Device parameter	1.2kV/50A	6.5kV/100A	15kV/500A	20kV/300A	20kV/600A	20kV/1500A
Efficiency	97	97.5	98	98.5	98.6	98.8

Table 3.5 Market proportion forecast of photovoltaic inverter using SiC devices

	2020	2025	2030	2035	2040	2048
Market proportion %	10	50	70	75	80	85

Note: other Si devices, GaN devices or other future power devices may be applied.

3.4.5 Solid state switches

3.4.5.1 Introduction

According to the power character of the application system, solid state switch (SSS) can be divided into AC SSS and DC SSS. According to the switching topology structure, it can be divided into pure SSS and hybrid switch. According to the type of device used, it can be divided into full-controlled SSS (with IGBT) and half-controlled SSS (with thyristor).

One of the applications of solid state switches in the high voltage field is the HVDC circuit breaker. There are three types of HVDC circuit breakers: mechanical HVDC circuit breakers, solid-state HVDC circuit breakers and hybrid HVDC circuit breakers. Solid-state HVDC circuit breakers employ pure power electronic devices as the main breaking device. Compared with the traditional mechanical circuit breakers, its dynamic performance advantage is obvious. Hybrid HVDC circuit breakers employ a hybrid topology of power electronic devices and mechanical switches. Both hybrid and mechanical HVDC circuit breakers have been tested and applied in engineering.

The applications of solid-state switches in low-voltage AC are mainly solid state relays and contactors, which are suitable for occasions requiring frequent switching and long service life. The output of Crydom AC solid-state contactor can be up to 150 Arms/ 660Vac.

The application of the solid state switch in transformers is the on-load tap-changer (OLTC), which include mechanical, hybrid and power electronic. Hybrid solid-state switches commonly employ thyristors or IGBTs, while power electronic solid-state switches usually employ IGBTs. If the OLTC is placed in the transformer, it is required that the OLTC could implement the corresponding switch operation when the oil temperature is 150 °C, which cannot be realized through Si devices.

3.4.5.2 Driving forces

The driving forces of SiC devices in solid state switches are (1), (2), (5), (6) and (7) in section 3.3.2. Reducing losses is mainly to reduce the on-state loss of power electronic devices in DC circuit breakers or power electronic OLTCs; special operating environment requirements are only limited to OLTCs in the transformer

box.

3.4.5.3 Requirements for device

- For DC circuit breakers, use press pack to ensure short circuit failure;
- For DC circuit breakers, high shutdown current capacity is required. When system fails, the circuit breaker valve will withstand a large current of 2-5 ms with the peak value above several tens of kA;
- For ordinary frequent switching switches, maximum voltage of single device should be greater than 10 kV;
- For ordinary frequent switching switches, good heat resistance is required to withstand the impact of the fault current;
- For OLTCs with 10 kV distribution transformers, the voltage of power electronic devices should not be lower than 1200 V and the rated current should not be smaller than 50 A;
- For OLTCs in the transformer box, the junction temperature of the device should not be less than 200 °C;
- For OLTCs in the transformer box, good sealing ability is required to work in the transformer oil for a long time.

3.4.5.4 Development forecast

- Within 5 years (up to 2023), high-voltage solid-state switches with 35 kV and above could be realized for the 3300-4500 V hybrid power module;
- The voltage and current of products based on SiC are relatively small, and the application of SiC is expected be first tested in the OLTC of the transformer.

Table 3.6 Development prediction of solid state switch

	2020	2025	2030	2035	2040	2048
Voltage level (AC)	0.4kV	10 kV	35 kV	±110 kV	±220 kV	±500 kV
Type	AC circuit breaker	AC circuit breaker or OLTC	AC circuit breaker or OLTC	DC circuit breaker	DC circuit breaker	DC circuit breaker
Current A	100	630	1200	2500	2500	3000
Device	MOSFET	IGBT	IGBT	IGBT	IGBT	IGBT
Device parameter	1.2kV/100A	15kV/650A	15kV/650A	20kV/1250A	20kV/1250A	20kV/1500A
Loss %	1.5	1	0.9	0.8	0.7	0.6

3.5 Technology routes of SiC devices in electric traction applications

3.5.1 Introduction

Rail transit vehicles show diversified development. From the running state of the

vehicles, they can be divided into trunk locomotives, urban rail vehicles and high-speed trains. Among them, trban rail vehicles and high-speed trains are the main driving forces for the future development of rail transit. Power semiconductor devices are widely used in rail transit vehicles. It can be said that the development of power semiconductor devices has promoted the development of rail transit. The traction converters, auxiliary converters, main and auxiliary integrated converters, power electronic transformers and power chargers all need SiC devices.

3.5.2 Driving forces

The development trend of green and intelligent rail transit demands higher speed and lower loss for high-speed rail transit, higher efficiency, smaller volume and higher power density for power electronic devices of rail transit vehicles, and higher working frequency and integration of the system. These require the support of new generation of devices.

3.5.3 Requirements for device

- Power electronic transformers require single device withstand voltage of more than 10 kV;
- The traction converter of trunk locomotive requires a single device withstanding voltage of 3300 V;
- High-speed train traction converter requires single device withstand voltage of 3300 V and 6500 V;
- The traction converter of urban rail transit requires single device withstand voltage of 1700 V and 3300 V;
- The short circuit capability of the device is larger than or equal to 10 us.

3.5.4 Development forecast

a) Applications of SiC devices in rail transit vehicles. From the category, vehicles mainly include main-line locomotives, bullet trains such as high-speed railway vehicles, metros and other urban rail transits, meglev trains and trams. With the process of urbanization and globalization, rapid growth of rail traffic vehicles will be expected, especially urban rail transits and high-speed railways. At present, there are about 120,000 urban rail transit vehicles (including metros and light railways), 8,000 high-speed railways and 75,000 main-line locomotives in operation; a small, negligible amount of maglev traffics which is just in its infancy; and other rail transit vehicles about 100 thousand.

b)

Table 3.7 Prediction of vehicles in various categories

Category	2018 (10,000)	2030 (10,000)	2040 (10,000)	2050 (10,000)
Main-line locomotives	7.5	10	11.5	12.5

High-speed railway vehicles	0.8	2.1	3.2	4
Metro and other urban rail transits	12	20	28	32
Maglev traffics	0.01	0.05	0.09	0.12
Other rail transit vehicles	10	15	18	20
Sum	30.31	47.15	60.79	68.62

b) Applications of SiC devices in rail transit vehicles, according to the device categories, can be divided into traction converters, auxiliary converters, main and auxiliary integrated converters, power electronic transformers, power chargers, etc. With the development toward green and intelligent of rail traffics, as well as the higher speed requirements of high-speed railways, power electronic devices with smaller volumes and higher power densities devices of rail transit vehicle are needed.

Table 3.8 Prediction of application devices in various categories

Category	2018 (10,000)	2030 (10,000)	2040 (10,000)	2050 (10,000)
Traction converters	403.58	537.42	556.56	600.6
Auxiliary converters	403.58	537.42	556.56	600.6
Main and auxiliary integrated converters	100.90	289.38	556.56	1115.4
Power electronic transformers	0.00	0.5	4	10
Power chargers	504.48	826.8	1113.12	1716
Sum	1412.54	2191.52	2786.80	4042.60

c) For the SiC devices in the application of rail transit vehicles, the improved function, space utilization efficiency and cost, increases the requirements for higher power intensities and smaller volumes. As a result, the power densities of traction converters, auxiliary converters, main and auxiliary integrated converters, power electronic transformers, power chargers and other power electronic devices will be continuously improved.

Table 3.9 Prediction of power densities of application devices

Category	2018 (kW/ L)	2030 (kW/ L)	2040 (kW/ L)	2050 (kW/ L)
Traction converters	2	5	10	30
Auxiliary converters	3	8	20	40
Main and auxiliary integrated converters	2	5	10	30
Power electronic transformers	1	2	4	8
Power chargers	5	12	22	40

d) For the SiC devices in the application of rail transit vehicles, with the

development of rail traffic toward green and intelligent, along with the need of cost reduction, the efficiency requirements for power densities of varies power electronic devices are constantly raised. The expected efficiencies of traction power converters, auxiliary converters, main and auxiliary integrated converters, power electronic transformers, power chargers and other power electronic devices will be continuously improved.

Table 3.10 Prediction of work efficiencies of application devices

Category	2018	2030	2040	2050
traction converters	93%	95%	97%	98%
auxiliary converters	95%	97%	98%	98.5%
main and auxiliary integrated converters	93%	95%	97%	98%
power electronic transformers	85%	90%	93%	95%
power chargers	95%	97%	98%	99%

e) For the SiC devices in the application of rail transit vehicles, the requirements for efficiencies of various power electronic devices are improved. With the demands for higher power intensities and smaller volume, the performance of power electronic devices used in traction converters, auxiliary converters, main and auxiliary integrated converters, power electronic transformers, power chargers and other power electronic devices should be continuously improved, and SiC devices will be gradually popularized.

Table 3.11 Prediction of various power electronic devices

Category	2018	2030	2040	2050
Si IGBT devices	98%	70%	30%	10%
Hybrid SiC devices	1%	17%	35%	30%
Full SiC devices	0%	5%	20%	40%
SiC discrete devices	1%	8%	15%	20%

f) For the SiC devices in the application of rail transit vehicles, the forms of heat dissipation of power electronic devices typically includes water cooling, forced air cooling, passive air cooling, etc. With the improvement of efficiencies of power electronic devices and the change of volumes, there are new changes and requirements on the form of heat dissipation.

Table 3.12 Prediction of varies heat dissipations

Category	2018	2030	2040	2050
Water cooling	55%	40%	22%	10%
Forced air cooling	40%	45%	35%	30%
Passive air cooling	5%	15%	28%	50%
Without radiator	0%	0%	5%	10%

g) For the SiC devices in the application of rail transit vehicles, the requirements

from terminal customers for the life of the power electronic devices in vehicles will be constantly raised.

Table 3.13 Prediction of service life

Category	2018	2030	2040	2050
8y	85%	36%	9%	0%
10y	15%	47%	31%	6%
15y	0%	16%	58%	88%
>20y	0%	1%	2%	6%

3.6 Technology routes of SiC devices in electric vehicle applications

3.6.1 Introduction

The electric vehicle industry is an emerging market with huge market in the future. The popularity of new energy vehicles is becoming clearer in the world. According to existing technical solutions, each electric vehicle uses power semiconductor devices ranging from about $700 to $1,000. With the development of electric vehicles, the demand for power semiconductor devices is increasing, which has become a new economic growth point of power semiconductor devices.

As shown in Figure 3.1, the components involved in power semiconductor applications in EV system architecture include: motor driver, on board charger (OBC), on-board DC/ DC and non-on-board charging pile.

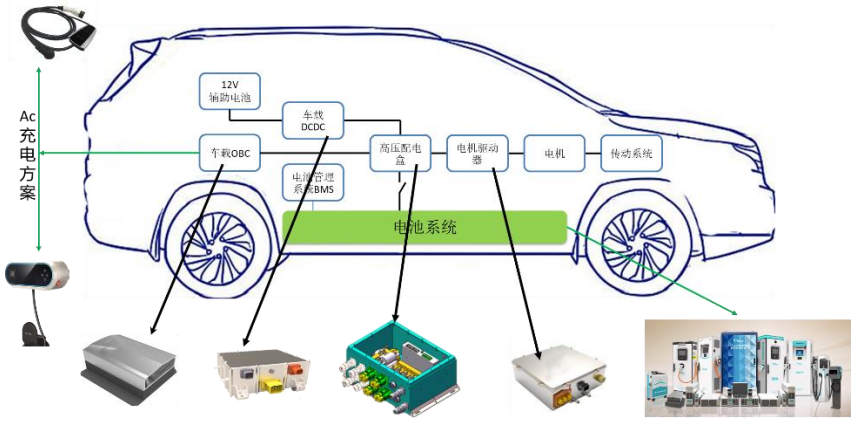


Figure 3.1 Electric vehicle and power electronic device

Currently, due to the good reliability and high efficiency, SiC devices have been popularized in onboard motor drivers, OBC and DC/ DC; while in the field of offboard chargers, SiC devices are not common because of the high cost. In the future, by taking full advantages of high voltage withstand and high frequency of SiC devices, the system-level cost will not only not rise, but also have a downward trend.

3.6.2 Driving forces of technology/ product development

The development of electric vehicles requires higher power, lower loss and smaller size of motor controllers. Therefore, the power density of motor controllers should be continuously improved from less than 10 kW/ L to 30 kW/ L, 60 kW/ L, or even 100 kW/ L. One of the most direct benefits of improving power density and efficiency of electric vehicles is to increase the mileage of electric vehicles. At the same time, the trend of integration of motor and controller requires higher speed of motors, higher working frequency and smaller size of controllers. These trends require SiC devices to play an active role in motor controllers. Specifically, the main driving forces come from the following aspects:

3.6.2.1 High voltage semiconductor devices with high power charging

Non-vehicle charging pile: At present, the charging power has raised to the power level of 350 kW. With the development of battery technology in the future, there will gradually be greater demand for charging power. One direction of high power is to increase the battery charging voltage, which will be an important application of the third generation semiconductor with high voltage characteristics.

3.6.2.2 High efficiency requirements from the pursuit of operational efficiency of the charging operation enterprises

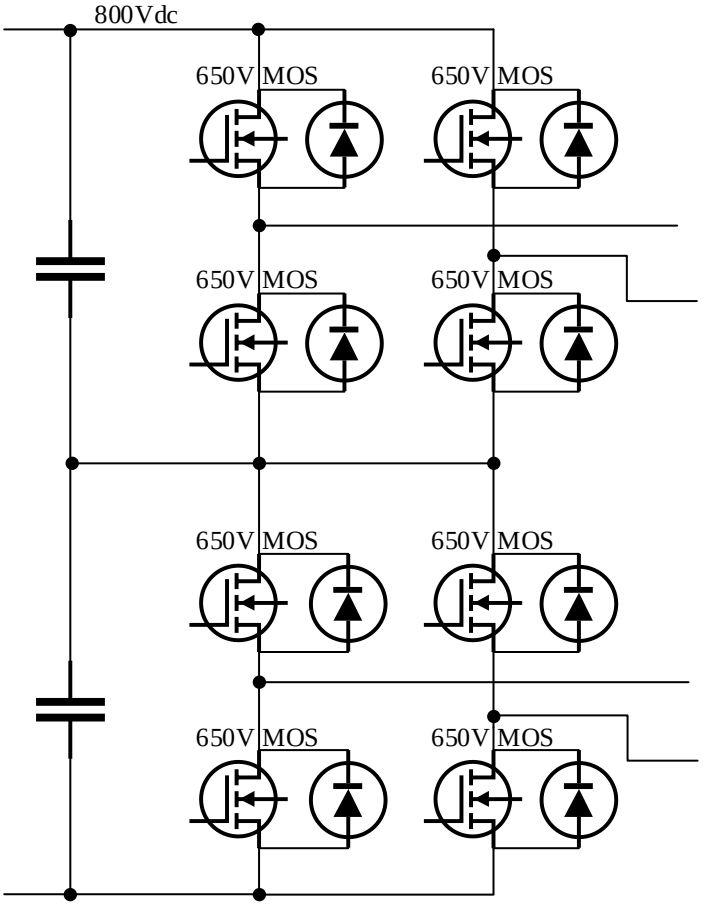
For the charging operation enterprises, the daily charging capacity is huge, and 1% efficiency improvement will bring huge operating cost reduction. At present, the system efficiency of Si-based semiconductor devices is about 96% for non-vehicle charging. The advantages of low on-loss and low switching loss of the third generation semiconductor will make the system efficiency reach 97% ~ 98%.

Table 3.6 Efficiency improvement of vehicle OBC and non-vehicle charging pile

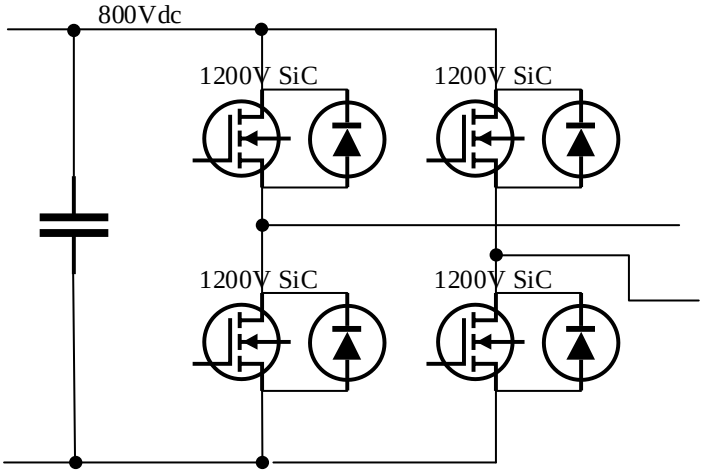
Year	Vehicle OBC	Non-vehicle charging pile (system)
2018	95%	96%
2048	97%	97%~98%

3.6.2.3 High voltage resistance and simplify topology requirements from high reliability requirements of vehicle products

For high voltage charging circuit topology, the existing design usually uses multi-level mode in DC/ DC topology, as shown in Figure 3.2. Full bridge three-level topology is used in the original side, and four pipes are needed in series for a single bridge arm. The circuit topology can be simplified as a full bridge topology with two tubes on a single bridge wall. The circuit topology and driving mode are greatly simplified.



a)Full bridge series topology



b)Common full bridge topology

Figure 3.1Circuit topology

3.6.2.4 High power density requirements from the lightweight demand for vehicle products and high frequency demand for non-vehicle products

For vehicle products such as motor controllers, OBC and other products, weight and volume are continuous requirements, also the core indicators of such products. The improvement of switching frequency is the key way to reduce product weight and

reduce product volume. In the future, the third generation of semiconductor and new energy vehicles will find a perfect match in the aspect of high frequency.

Table 3.7 Vehicle and non-vehicle converter switching frequency

	Vehicle		Non-vehicle	
Year	PFC	DCDC	PFC	DCDC
2018	25~50kHz	<200kHz	25~80kHz	80~300kHz
2048	150kHz	500kHz	150kHz	500kHz

3.6.2.5 High efficiency requirements for motor drives and DC/DC from energy efficiency indicators of electric vehicles

The charging industry has higher requirements for the conversion efficiency, standby power consumption and power density of the power module. The SiC devices have high switching speed and low switching loss, which is suitable for high frequency applications. With the maturity of SiC device technology and the decrease of cost, the application of SiC devices in charging module will be a trend in the future.

In the field of electric drive, the driving force of SiC devices mainly comes from the improvement of controller efficiency, power density and switching frequency. As shown in Figure 3.3, for a 90 kW rated controller, a 1200V/400A Si IGBT and a SiC MOSFET module are used to compare the drive efficiency.

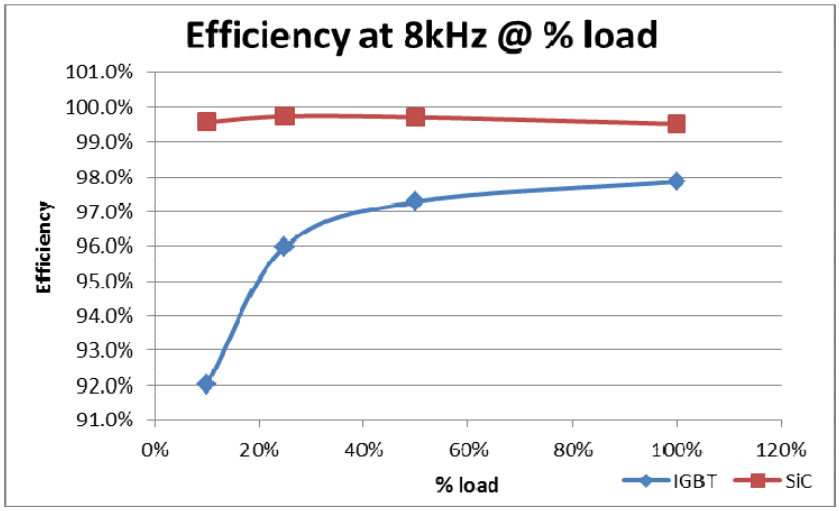


Figure 2.3 Efficiency comparison betweem Si IGBT and SiC MOSFET controllers

From figure 3.3, the application of SiC MOSFET improves the controller efficiency by 2% to 8%. According to NEDC standard working condition, the main contribution to energy consumption of electric vehicles is low load working condition. At this time, the advantage of SiC MOSFET is more obvious. Preliminary calculations show that the application of SiC MOSFET will bring about 5% efficiency improvement under comprehensive working conditions. The electric vehicle consumption is reduced by 1 kWh/ km, and the cost of the battery can be saved by about 1500 yuan. For long-range electric vehicles, such as the use of Si MOSFET, the reduction in battery costs can completely cover the increase in costs from Si IGBT to SiC MOSFET.

Secondly, due to the small size, low heat dissipation requirements, high junction temperature and other characteristics of SiC devices, they can help to reduce the volume of the electric drive controller by more than 80%. It is the inevitable choice of the controller power density to 50 kW/ L.

Finally, since the SiC MOSFET has lower switching loss, and the switching frequency can be raised to 20 kHz or higher, which will help to eliminate the noise of the drive system and improve occupant comfort.

3.6.3 Requirements for device

Vehicle charger requires 1200V SiC Schottky diode and MOSFET.

The motor controller of passenger car requires SiC MOSFET and diode device withstand voltage of 750V.

Commercial vehicle motor controller requires SiC MOSFET and diode device withstand voltage of 1200V.

Table 3.8 Requirements for vehicle and non-vehicle devices

Application area		Device	Voltage	Current
OBC		SiC SBD、SiC MOSFET	650V~1200V	≥20A
DC/DC		SiC SBD、SiC MOSFET	650V~1200V	≥20A
Electric drive	Passenger car	SiC MOSFET	650V~1200V	≥100A
	Commercial car	SiC MOSFET	1200V~1700V	≥100A

3.6.4 Key indicators/ parameters development trend

Overall, the development trend of new energy vehicles in power electronics related components is as follows:

Vehicle: lightweight, high efficiency, high reliability, high voltage, high current and high integration.

Non-vehicle: high voltage, high current, high power and high efficiency.

3.6.4.1 High voltage and high current

Because of the users' demand for charging speed and endurance mileage, the battery capacity of electric vehicles is increasing, and charging time will be shorter and shorter. The direct requirement is that the charging power is increasing. Therefore, in order to meet the requirements of high-power charging, the battery charging voltage will gradually develop from the current minimum 300 V to the highest 1000 V level. By 2048, in order to pursue faster charging, longer range, charging voltage can reach 1500 V. The maximum current will probably reach 800 to 1000 A, far exceeding the current 400 A.

3.6.4.2 Conversion efficiency

After the popularization of new energy vehicles, the annual power consumption of

the entire electric vehicle will be a huge number, and the automobile will become a high-energy-consuming industry. In order to save energy and protect environment, the power consumption of electric vehicles per 100 km becomes the concern of the main engine manufacturers and users, like the fuel consumption of traditional automobiles per 100 km. Currently, the conversion efficiency of vehicle OBC, DC/ DC and non-vehicle chargers varies from 93% to 97%. By 2048, the conversion efficiency of on-board power supply will exceed 98%.

3.6.4.3 Lightweight

Lightweight design is an important way to reduce energy consumption of electric vehicles, and it is also one of the most concerned indicators of all vehicle product developers. For power electronic products, the most important method to achieve small size and lightweight design is high frequency design, which makes the volume and weight of magnetic devices and capacitors greatly reduced. At present, the highest frequency of vehicle products is between 100 kHz and 200 kHz. With the breakthrough of devices and technology, the switching frequency of soft-switching circuit of vehicle products may exceed 500 kHz by 2048.

3.6.4.4 Heat dissipation

In terms of heat dissipation, SiC devices have less loss, lower mesa temperature rise, and more advantages for system heat dissipation. On the other hand, SiC has strong temperature tolerance. It is necessary to further optimize and enhance the temperature tolerance of packaging materials, so that the highest junction temperature of SiCdevices can be further raised to 200 °C, or even 250 °C.

3.6.4.5 Packaging format

In order to take advantages of SiC, the packaging of SiC devices for new energy vehicles will have the following trends:

(1) OBC and DC/ DC: ordinary TO series packaging (mainly to-247) → four-pin TO series packaging → small size SiC power module;

(2) Electric drive: ordinary plate or direct heat dissipation power module → double side heat dissipation power module;

(3) Packaging process: back ordinary welding process + front binding process → double-sided welding process → double-sided nano-silver sintering process.

3.6.4.6 Packaging format

For the new energy vehicles, the charging speed, range, reliability and economy need to be improved. Specifically, the improvement of the third generation semiconductor devices in new energy vehicles includes:

- Cost: Speed up the reduction of device cost through product yield and process simplification; optimize the circuit structure and system performance by SiC devices to reduce system costs;
- Reliability: Improve device reliability by drive and packaging technology;
- Charging speed: Achieve more power design by continually increasing device voltage withstand (greater than 1500 V) and current carrying capacity;
- With the increasing charging power, the packaging of discrete devices will certainly not meet the needs of the industry. So multi-transistor packaging, full-topology packaging and composite packaging for higher power need to

be introduced as soon as possible.

Figure 3.4 SiC application prediction

- In the field of electric drive, there are certain requirements for threshold voltage of SiC MOSFET. The corresponding threshold voltage needs to be increased from over 2.0 V to over 4.0 V.

3.6.5 Development forecast

According to the characteristics of SiC devices and the development trend of electric vehicles, SiC devices are the inevitable choice for future electric vehicles. By solving the problems of cost, drive, EMI caused by high frequency and diode surge protection, SiC devices can be widely and fully developed in the vehicle charging part of electric vehicles. By optimizing the circuit topology and increasing the operating frequency of the system, using SiC devices can further enhance the power density of the motor controller, and can form an integrated structure of the motor and the driver to promote the development of electric vehicles.

Table 3.9 Development prediction for electric vehicle motor drive using SiC devices

	2020	2025	2030	2035	2040	2048
Voltage level (DC)	500V	750V	900V	1.2 kV	1.5 kV	2 kV
Capacity kW	60	100	150	200	250	300
Device	MOSFET	MOSFET/IGBT	MOSFET/IGBT	MOSFET/IGBT	MOSFET/IGBT	MOSFET/IGBT
Device parameter	1.2kV/30A	1.7kV/50A	2kV/50A	2.5kV/100A	3.3kV/100A	4.5kV/100A
Efficiency	97	97.5	98	98.5	98.6	98.8
Power density (kW/L)	50	80	100	120	150	170

Table 3.10 Development prediction of electric vehicle charging facilities using SiC devices

	2020	2025	2030	2035	2040	2048
Voltage level (DC)	500V	750V	900V	1.2 kV	1.5 kV	2 kV
Capacity kW	60	100	150	200	250	300
Device	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET
Device parameter	1.2kV/30A	1.7kV/50A	2kV/50A	2.5kV/100A	3.3kV/100A	4.5kV/100A
Efficiency	95	96	96.5	97	97.5	98

Power density (kW/L)	50	80	100	120	150	170

3.7 Technology routes of SiC devices in household appliances and consumer electronics

3.7.1 Introduction

At current, there two major trends in the development of the global household appliance and consumer electronics industries: First, green and low-carbon, and second, focusing on user's need. Among them, energy-efficient has become an important direction for the future development of electronic products. Power consumption standard has been gradually implemented in the world, and more and more countries will adopt the green power standards.

The consumer electronic products typically include two categories: one is the static switching power supply products, such as LED driving powers, power adapters, induction heating and micro-inverters; the other is the motor driving power, for example, air-conditionings, refrigerators and washing machines. Detailed classification is given in Figure 3.4.

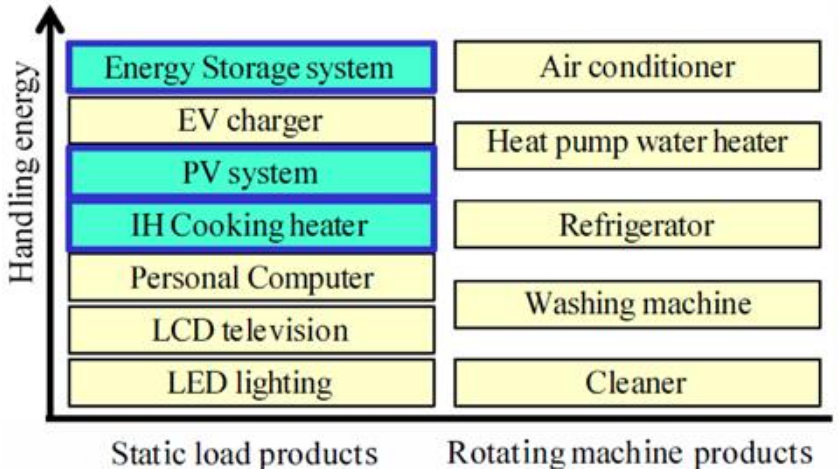


Figure 3.4 Classification of household consumer electronic products

3.7.2 Driving forces of SiC devices in household consumer product applications

The driving forces for SiC devices (including hybrid SiC devices) in household consumer product applications are (1), (5) and (6) in section 3.3.2.

In the *Comprehensive Work Plan for Energy Conservation and Emission Reduction in the 13th Five-Year Period* issued by the State Council, the promotion of energy-saving appliances has become an important aspect of energy conservation and emission reduction. It is estimated that by the end of the 13th Five-year Period, the energy-saving and environmental protection level of China's major household

appliance products will approach the international advanced level, and the energy efficiency levels of major household appliance products will increase by 15% on average. *Development Guidance for Chinese Household Appliance Industry in the 13th Five-Year Period* also pointed out that technological innovation, energy saving and environmental protection will be the key words of appliance industry upgrade; China has started to address energy efficiency requirements for household and consumer electronic products, as well as energy labeling for products like refrigerators, air conditioners and washing machines.

Figure 3.5 shows the American energy efficiency standard requirements for adapter power products [12].

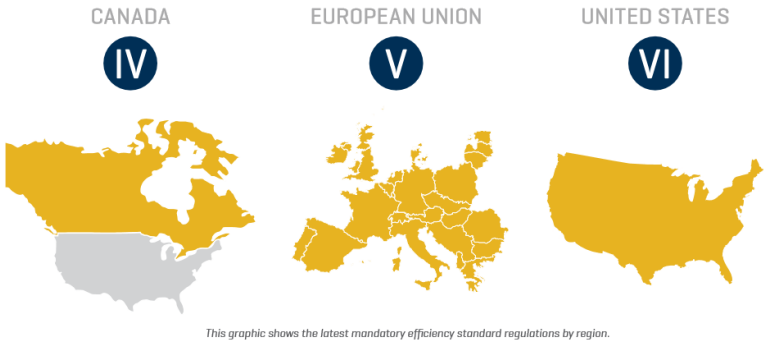


Figure 3.5 Energy efficiency standard requirements for adapter power products

Table 3.19 shows the latest energy efficiency standard requirements mandated by major European countries and the United States. The US Department of Energy (DOE) issued in 2014 and implemented the new level VI efficiency requirement in February 2016: Regulators further improved efficiency standards for external power supplies. Since 2018, there will be more strict requirements in Europe, and the current voluntary requirements for external power supplies will become mandatory. In addition, European countries and the United States have direct requirements for consumer electronic products. Therefore, if products from China are to be exported to Europe and the United States, the energy efficiency requirements must be met.

From the perspective of market regulation, more and more stringent requirements on the standby power and the efficiency are implemented around the global. Improving the efficiency and reducing the standby power have been two key indexes of consumer electronics and appliances. And these requirements for increased efficiency will provide greater market momentum in the power device field.

Table 3.19 The latest energy efficiency standard requirements imposed by major European countries and the United States

Level	No-load Power Requirement	Average Efficiency Requirement
I	used if you do not meet any of the criteria	
II	no criteria was ever established	no criteria was ever established
III	≤10 Watts: ≤0.5W of No Load Power 10~250 Watts: ≤0.75W No Load	≤1Watt: ≥Power×0.49 1~49 Watts: ≥[0.09×Ln(Power)]+0.49

	Power	49~250 Watts: ≥84%
IV	0~250 Watts:≤0.5W No Load Power	≤1Watt: ≥Power×0.50 1~51 Watts: ≥[0.09×Ln(Power)]+0.5 51~250 Watts: ≥85%
V	Standard Voltage AC-DC Models (>6 Vout)	
	0~49 Watts: ≤0.3W of No Load Power	≤1Watt:0.48×Power+0.140
	50~250 Watts: ≤0.5W of No Load Power	1~49 Watts:[0.0626×Ln(Power)]+0.622
		50~250 Watts:≥87%
	Low Voltage AC-DC Models (<6 Vout)	
	0~49 Watts: ≤0.3W of No Load Power	≤1Watt:0.497×Power+0.067
	50~250 Watts: ≤0.5W of No Load Power	1~49 Watts:[0.0750×Ln(Power)]+0.561
		50~250 Watts:≥86%

3.7.3 Development trends of SiC in household appliance and consumer product applications

Figure 3.7 shows the distribution of power consumption of different household electronic products [13]. According to Mitsubishi Electric, in the power consumption list of household consumer electronics, air conditioning ranks first, accounting for the 53% of total power consumption; followed by refrigerator, accounting for 23%; and the least are television, lighting and others. It is seen that the power consumption of air conditioning and refrigerator account for 76% of the total electricity consumption of household appliances. Therefore, it is of great significance and market potential to develop energy-saving technologies for traditional appliances such as air conditionings and refrigerators. Utilizing the material characteristics of wide bandgap semiconductors like SiC and GaN could greatly reduce the loss of the entire power converter and hence improve the energy efficiency.

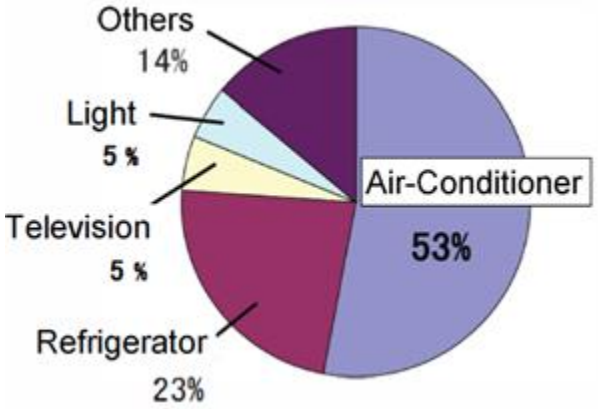


Figure 3.7 Power consumption distribution of different household electronic

products

The electric control system of air conditionings utilizes the inverter to convert the power frequency power to voltage and frequency controllable power to provide reliable power supply for air conditioning compressors. Electric control system mainly adopts the AC-DC-DC mode: The AC power is converted to DC power through the rectifier first, and then the DC power is further converted to frequency and voltage controllable AC power and supplied to the motor. The entire control circuit is usually composed of 4 parts: rectification, DC intermediate link, inverter and control. The internal control circuit of the air conditioning electrical system is shown in Figure 3.8 [13].

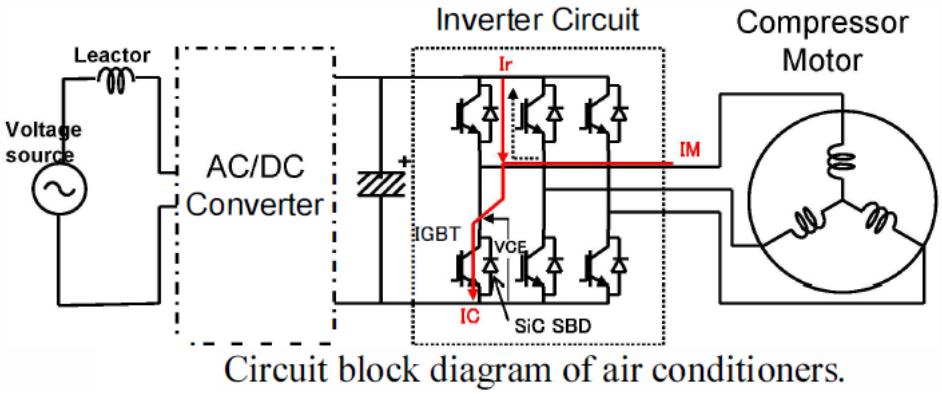


Figure 3.8 Block diagram of air conditionings electrical control system

Although SiC devices have obvious performance advantages, the price of SiC devices is relatively higher than that of traditional Si devices. Based on the consideration of the reliability of SiC MOSFET switching devices and the price sensitivity, Si IGBT + SiCdiode hybrid power module is a cost-effective solution adopted in current household appliances. Figure 3.9 shows the SiC hybrid power module.

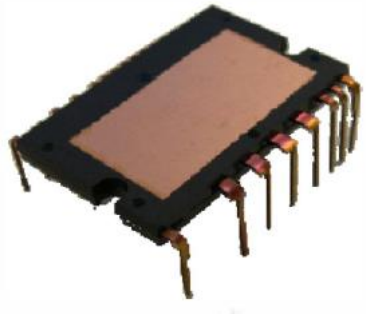


Figure 3.9 SiC hybrid power module

The good reverse recovery characteristic of the SiC diode is able to greatly reduce the switching loss of the diode itself, and greatly reduce the turn-on loss of the IGBT meanwhile. By employing the SiC hybrid power module, the switching loss of the entire air conditioning driving system is reduce by 60%. It not only improves the energy efficiency of the air conditioning, but also reduces the cost of the heat dissipation. Figure 3.10 shows a comparison of turn-on voltage/ current waveforms.

Table 3.20 gives the comparison of the switching loss of SiC hybrid power modules [13].

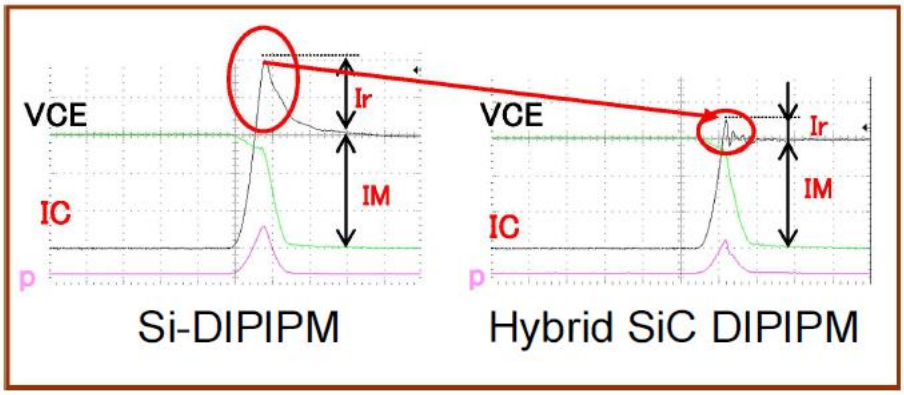


Figure 3.10 Comparison of turn-on voltage/ current waveforms

Table 3.20 Comparison of the switching loss of SiC hybrid power modules

	HybridSiC DIP IPM	Power loss improvement rate
	%	%
IGBT turn-on loss	43	57
FRD turn-on loss	25	75
Switching loss	40	60

With the maturity of SiC MOSFET manufacturing process and the cost reduction, SiC MOSFETs are expected to replace Si IGBTs and become the mainstream switching power devices in the future. The full SiC power module is the future development trend of hybrid power modules, proving the technical feasibility of miniaturization and high efficiency of future household consumer electronic products. Figure 3.11 shows the development trend of the power module in the future.

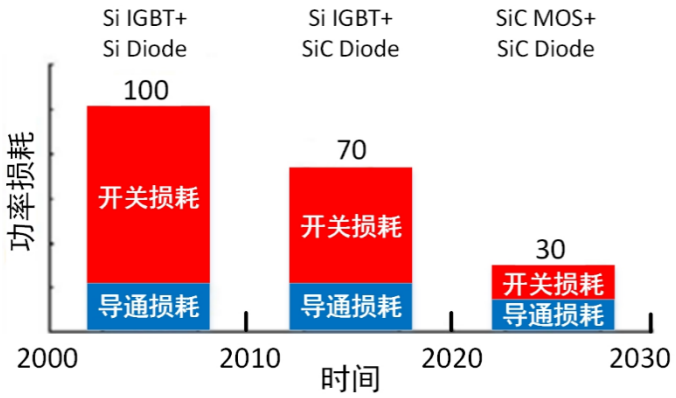


Figure 3.11 Development trend of power modules、

Table 3.11 Prediction of household appliances and consumer electronics using SiC power module

	2020	2025	2030	2035	2040	2048
Power	Hybrid (Si	Hybrid (Si	Full SiC	ullSiC (SiC	ullSiC (SiC	ullSiC (SiC

module	IGBT+SiC Diode)	IGBT+SiC Diode)	(SiC MOS)	MOS)	MOS)	MOS)
Device parameter	650V/20A	650V/30A	650V/20A	650V/25A	650V/30A	650V/30A
Efficiency	95.5%	96%	96.5%	97%	97.5%	98%
Component proportion %	50%	50%	100%	100%	100%	100%

3.8 Summary

Environmental protection, economic benefits and the demand for practical applications are the three factors of promoting the development of energy-saving technology. As the demand for energy conservation gradually increases, SiC technique is effective in reducing the power consumption of the device and improving the efficiency of other parts of the system directly or indirectly. During the transfer and use of energy, SiC technique plays a role in monitoring, adjusting, optimizing and controlling, achieving more efficient, energy-saving and environmental friendly use of energy.

The development and application prospect of SiC devices is extremely broad. Their applications are expanding from traditional industrial-control area, such as computers, communications, consumer electronics and automotive electronics, to every aspect of national economy and national defense construction. In the future, power devices made by SiC materials will support the development trend of energy-saving technology and become the core components of energy-saving devices. Therefore, SiC power devices are acclaimed as the CPU of converters and the core of the green economy.

With the maturity of SiC production process and declined cost, new intelligent power modules (IPM) mainly based on SiC power devices become more and more widely applied in household electric appliances. Compared with common IGBT modules, SiC hybrid power modules significantly improve the performance and reliability of the system. Due to the low switching loss of SiC power modules, the size of the radiator and the whole system of are reduced, leading to a good economic efficiency and promising development prospect. The whole SiC power module can be researched as the core module of the future energy-saving electronic products.

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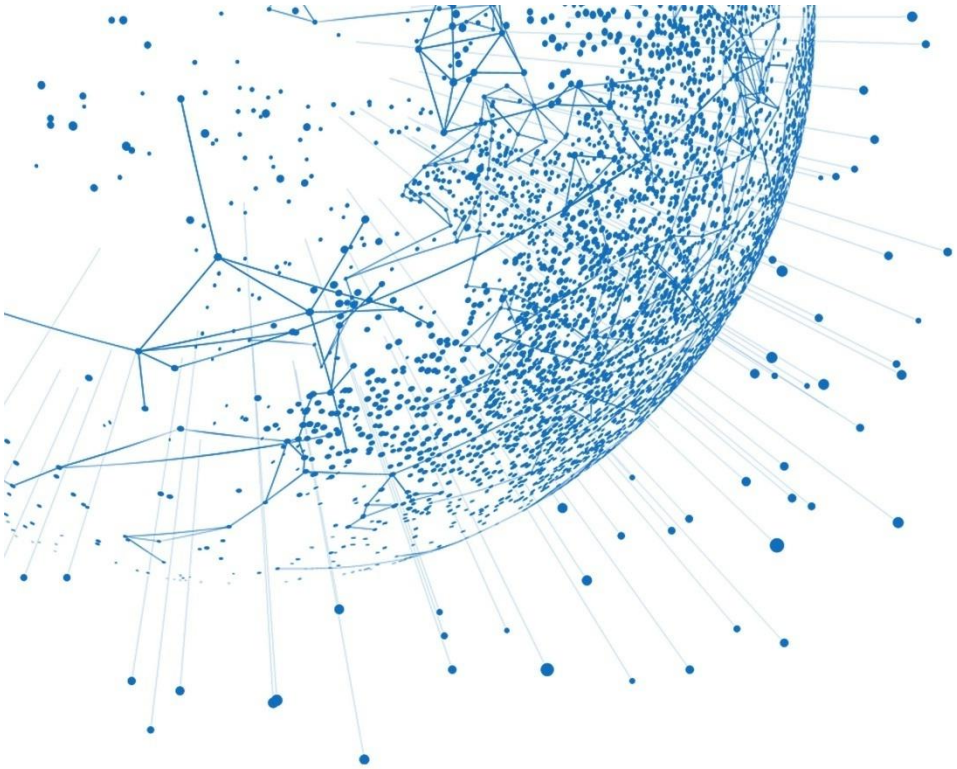


GaN Applications

4.1 Introduction

With the continuous development of semiconductor technology, the performance of silicon power metal oxide semiconductor field effect transistor (MOSFET) has reached the theoretical limit of Si material. Although super junction (SJ) MOSFETs further improve the performance of Si MOSFETs by improving the doping process, the performance improvement is limited by the physical properties of Si materials.In recent years, devices based on gallium nitride (GaN) materials have developed rapidly, and as a new generation of semiconductor materials that has emerged in the past 20 years, it has many advantages in performance. Compared with Si materials, GaN materials have many advantages, such as wide band gap, high melting point (high temperature resistance, radiation resistance), high breakdown voltage, high voltage resistance, fast electron saturation drift (high frequency operation), and high thermal conductivity, which makes GaN devices more suitable for high temperature, high voltage and high frequency applications.

Due to the material properties of GaN, GaN-based devices have many excellent properties in their applications:

- High voltage withstand capability enables the size reduction of device materials at the same voltage, making them suitable to replace Si devices which need to be in series for high voltage resistance applications, and perform better in high voltage applications.
- For GaN, a heterostructure can be utilized to realize two-dimensional electron gas, improving the carrier mobility and adjusting its concentration, thereby reducing the on-resistance and the parasitic capacitance, and increasing the operating frequency;
- The wide bandgap and the stable material property is conducive to high temperature work.

At present, GaN transistors on the market can be classified into the depletion mode and the enhancement mode. Early GaN transistors were mostly depletion mode. And this type of GaN transistor exhibits a normally-on characteristic and requires a negative voltage between the gate and source to be turned off. Since the level of its driving voltage is incompatible with the level of a conventional driving chip, its application is inconvenient. The enhancement GaN transistor exhibits a normally-off characteristic. When the voltage level between gate and source is high, the switch is turned on; when the voltage level is low, the switch is turned off. The level of its driving voltage is compatible with the level of a conventional driving chip. In view of the safety of shut-off and the compatibility with current systems in practical applications, the normally-off device is required for practical applications.

4.1.1 Cascode GaN transistors

In 2013, Transphorm Inc. introduced the first Cascode GaN transistor. As shown in Figure 4.1, it cascades a high-voltage depletion GaN transistor with a low-voltage Si MOSFET, and control the on/off of the entire device through controlling the on/off of the low voltage Si MOSFET, thus realizing the normally-off function of the device. Transphorm's Cascode GaN transistor products are high voltage series, mainly including 600V and 650V voltage levels. In medium and high voltage applications, the mainstream product is the Cascode GaN transistors, which guarantees fast switching speeds. And its driving level is in consistent with conventional MOSFETs. However, due to the cascading of the low voltage Si MOSFET, there is a reverse recovery loss when the switch is turned off, which limits the further improvement of the switching frequency. Currently, Cascode GaN transistors have a switching frequency of approximately 300k - 1MHz.

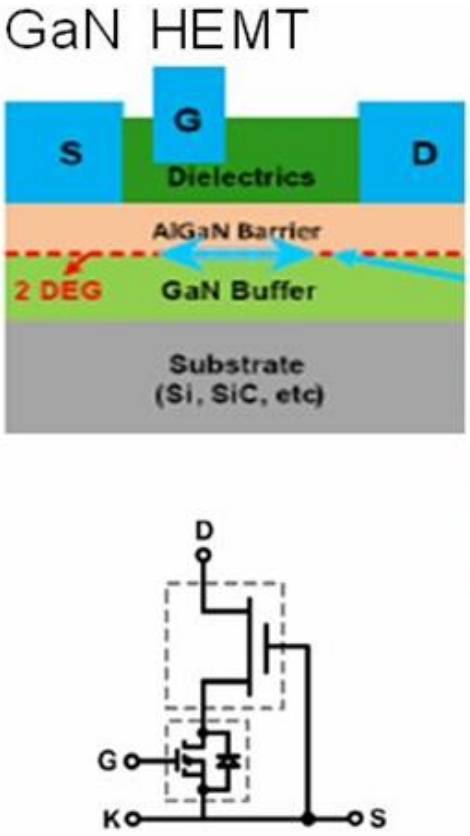


Figure 4.1 Cascode GaN transistor

4.1.2 P-gate GaN transistors

At present, there are several companies are able to offer p-gate normally-off GaN transistors, such as EPC, GaN System, Panasonic, and Visicof Israel, etc. Among them, EPC first realized the commercialization of p-gate structure device. The

products of EPC are low voltage series, with voltage levels of 15V, 40V, 80 V, 100V, 200V and so on.The packaging form mainly includes LGA and BGA, which are advantageous for reducing parasitic parameters of the switch tube and further realizing high frequency of the device. Currently, after being updated for many times, the GaN products of EPC have been leading in the industry. Taking EPC2016 as an example, table 4.1 gives its electrical parameters [14].Monolithic GaN transistors have the following advantages:1) the gate charge Qg of the transistor is extremely low, which is conducive to reducing the drive loss; 2) there is no bulk diode in the transistor, and its reverse recovery charge Qrr is zero, so there is no reverse recovery problem; 3) the transistor is packaged in a land grid array (LGA), as shown in Figure 4.2 [14].The drain and source are staggered to reduce the parasitic inductance of the leads. It is worth noting that the monolithic GaN transistor has a narrow driving voltage range and a low threshold voltage. In high-frequency, medium and low voltage applications, the parasitic inductance in the drive circuit will resonate with the gate-source junction capacitor, resulting in high-frequency oscillations of the driving voltage, which may lead to the false triggering of the transistor, or even breakdown of the gate and source of the transistor. This will pose a serious challenge to the design of the driving circuit.

Table 4.1 Electric parameters of EPC2016

型号	vds/ V	Id/A	Qg/n C	Qrr/n C	Vth/ V	vgs/V	封装
EPC2016	100	11	3.8	0	1.4	–5 ~ 6	LGA

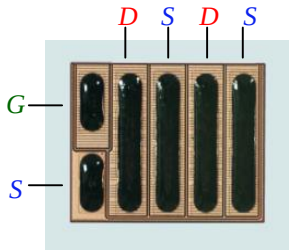


Figure 4.2 Schematic diagram of LGA package

4.1.3 Insulatedgate structure GaN transistor

At present, the most common use of the insulated gate is the groove gate structure, as shown in Figure 4.3 [14].The working mechanism is to cut the 2DEG under the gate through the groove, so that the device is turned off at zero gate voltage. When the positive gate voltage increases, an electron accumulation layer will gradually form at the interface between the dielectric layer and the semiconductor as the conductive channel of the device, leading to the conducting state of the device. Currently, a lot of research work about fabricating normally-off device through the groove insulated gate technology has been reported at home and aboard. The insulated gate has the

advantages of suppressing gate leakage and enhancing gate swing. However, there typically exists high density (10^{12}-$10^{14}$$cm^{-2}$ eV^{-1}) shallow and deep level trap states at the insulated gate-dielectric/semiconductor interface. The asynchronism of the dynamic charging/discharging behavior of these trap states may lead to the instability of the threshold voltage. The reliability problem of the industrialization of insulated gate devices has not yet been effectively solved. In general, the industry is expecting a normally-off device with a groove gate structure, which is able to solve problems caused by p-gate structure and Cascode structure. However, there is no definite solution for the stability of threshold voltage of the insulated gate structure device, and there is no commercialized product.

(c)凹槽绝缘栅结构

Figure 4.3 Groove grid structure GaN FET

Over the past two years, integrated devices have gradually emerged, such as Navitas, Dialog and so on. Generally speaking, GaN devices represent a new development direction of power electronic devices. Its excellent characteristics promote the development of power electronic converters continuously. GaN devices will compete strongly with Si-based power electronics.

4.2 Application areas

4.2.1 Overview of GaN applications

High frequency, high efficiency and high voltage resistance enable GaN devices to be widely available in many fields. The current voltage range of GaN lateral devices is below 650V. In the voltage range of 0-650V,Si-based power devices are still very competitive. GaN is still difficult to compete directly with Si devices in terms of industry acceptance, system maturity, peripheral device matching, device and system cost.

At this stage, the way GaN enters the market is usually in areas where GaN devices can give full play to their performance advantages while Si devices cannot achieve, or where the additional value of performance can be accepted by customers. Up to now (mid 2018), the application industry of GaN is still relatively small. Compared to conventional Si MOSFETs, the switching speed of GaN switching

devices is at least 10 times fast in theory, which make them perform better in some high frequency fields. The third generation semiconductor chip can eliminate 90% of the energy loss of the rectifier during AC/DC conversion, and can also reduce the volume of the notebook power adapter by 80%.

Compared with Si-based superjunction MOSFET devices, the advantages of GaN devices under hard-switching conditions are not obvious, while the performance under soft-switching conditions has been significantly improved. The reason is that the switching delay of GaN devices is very short, the conduction loss and switching loss are low, and the operating frequency is high. Advantages of GaN devices are mainly in low voltage (0-400 V), high frequency applications, and areas requiring high efficiency or miniaturization, such as ITC power supplies, notebook computer adapters and some high-frequency applications including laser radar drives, high frequency wireless charging, envelope tracking, etc.

1) Class D audio power amplifiers. The shortening of the rise time and the fall time during the switching process is beneficial to improve the analog bandwidth of the audio amplifier, thereby reducing the distortion of the sound signal and maintaining the maximum assurance for the original sound.
2) Resonant wireless charging adapters. Take the Class E switch mode amplifier technology route as an example. It not only requires a switching frequency of the power switching device as high as 6.78 MHz, but also requires the device to withstand a voltage as high as 200 V.
3) Communication and data center power supplies. Electricity charges rank the top five in the data center operating costs. No reverse charge recovery effect, low switching loss and other material properties enable GaN devices improve the efficiency of power supply by 1%.
4) Consumer electronics. Consumer electronics have a strong demand for miniaturization and low heat. The switching frequency of the GaN device is at least 3 times that of the Si-based super junction MOSFET device with the same parameters. With the totem-pole PFC and LLC resonant soft switching technology, the power density of the switching power supply based on GaN devices can be increased by two times.
5) Aerospace power supplies. The tolerance of irradiation dose of GaN devices is much better than that of Si devices. In addition, aerospace power supplies also have a strong demand for miniaturization and lightweight.

Other applications are also being developed, such as high-efficiency and lightweight on-board-chargers (OBCs). Figure 4.4 is a forecast by IHS, a market consultancy, of the main possible future applications of GaN-on-silicon power devices.

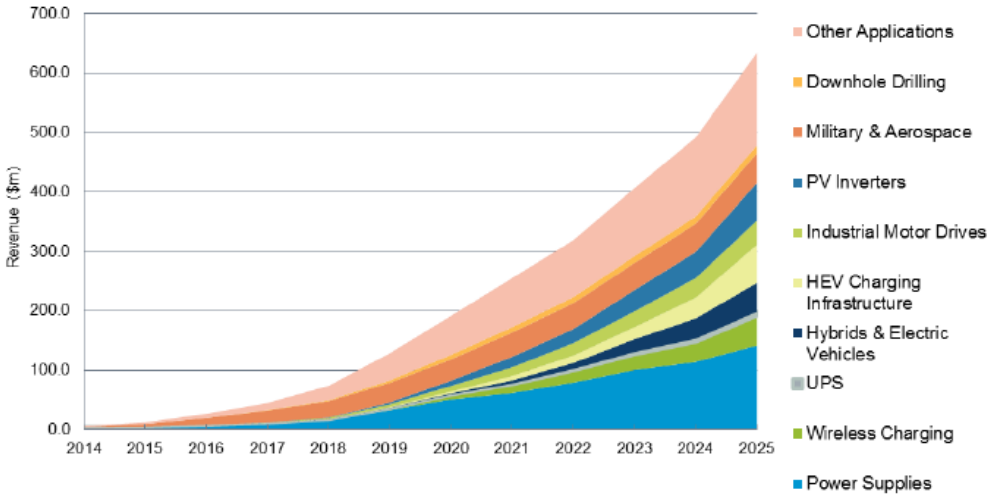


Figure 4.4 Applications and market share of GaN power devices (source: IHS)

4.2.2 Server power supply applications

With the rapid development of global information technology, the amount of computer data processing increases rapidly, and the capacity of data centers of various network operators has been expanding day by day. As the key equipment of a data center, the demand for servers has increased year by year, and the energy consumption problem has become increasingly prominent. How to improve the power utilization efficiency of the server system is becoming more and more important.

The server is generally powered by DC. Figure 4.5 shows the architecture of the distributed server power supply system [15]. The system consists of a power factor correction (PFC) converter, an intermediate bus converter and several point of load (PoL) converters. Among them, the PFC converter converts the mains into a stable high-voltage DC bus voltage and realizes power factor correction simultaneously; the intermediate bus converter converts the high-voltage DC bus voltage into a low-voltage DC bus voltage and realizes electrical isolation at the same time; and different PoL converters convert the low-voltage DC bus voltage to the required DC voltage, supplying corresponding DC load. The intermediate bus converter is an important part of the distributed power system. In order to improve the conversion efficiency of the server power supply and reduce its size, it is necessary to develop intermediate bus converters with high efficiency and high power density.

Figure 4.5 Structure of distributed server power system

Figure 4.6 shows the main circuit structure diagram of the intermediate bus converter [15] as an application case.Its switching frequency is set to 500kHz.The

converter adopts LLC resonant converter, and the primary side adopts full bridge circuit; because of the large output power and high switching frequency, the main transformer is divided into two parts, and the primary side is connected in series while the secondary side is connected in parallel, so the voltage sharing of the primary side winding and the current sharing of the secondary side winding can be realized automatically; the secondary side of the converter adopts a full bridge rectifier circuit, so that only one winding is needed for the secondary side of each transformer module, which simplifies the winding structure and is beneficial to the coupling of the primary side and the secondary side, and reduce the leakage inductance; considering the large output current of the converter, in order to reduce the conduction loss of the rectifier circuit, the synchronous rectification technology is used. The main technical indicators or the prototype are as follows:

- Input voltage: Vin = 380 V;
- Output voltage: Vo = 54.5 V;
- Output power: Po = 2 kW;
- Switching frequency: fs = 500 kHz;
- Size: 220 mm * 75 mm * 20 mm (length * width * height).

Among them, the primary switching tube of the converter uses the GaN device Cascode with a rated voltage of 600 V, a rated current of 12 A@100°C, and a package of TO-220. The photo of the prototype is shown in Figure 4.7 [15]. The height of the prototype is only 20 mm, one-half the height of the existing mainstream products at the same level, which improves the power density of the converter. Figure 4.8 presents the efficiency curve of the converter [15]. At the switching frequency of 500 kHz, the maximum efficiency of the LLC converter is about 97.4%.

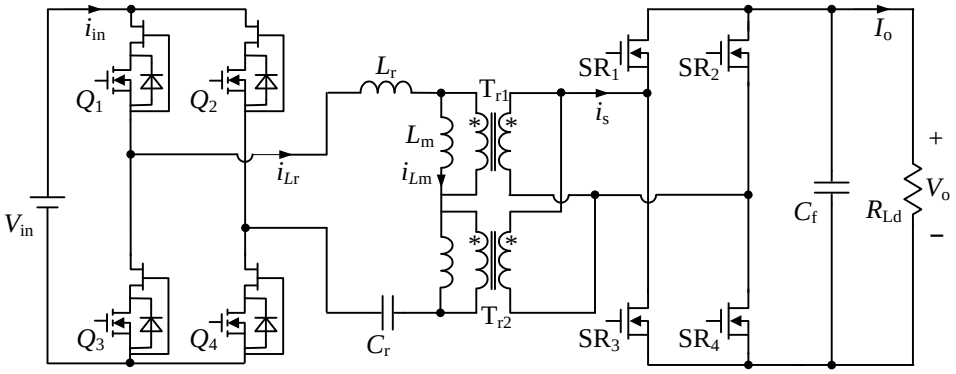


Figure 4.6 Main circuit structure diagram of the prototype

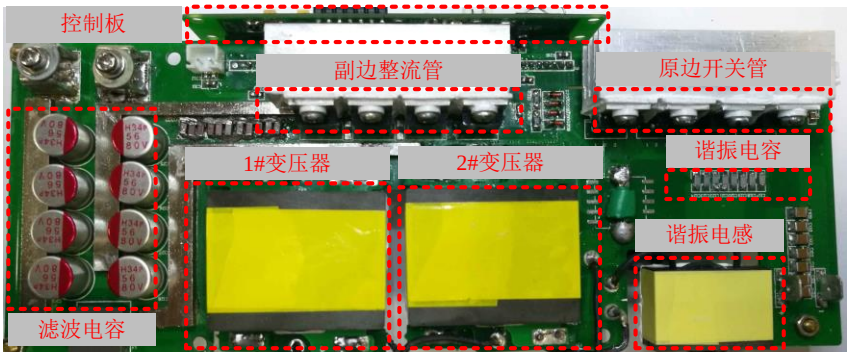


Figure 4.7 Photo of the prototype

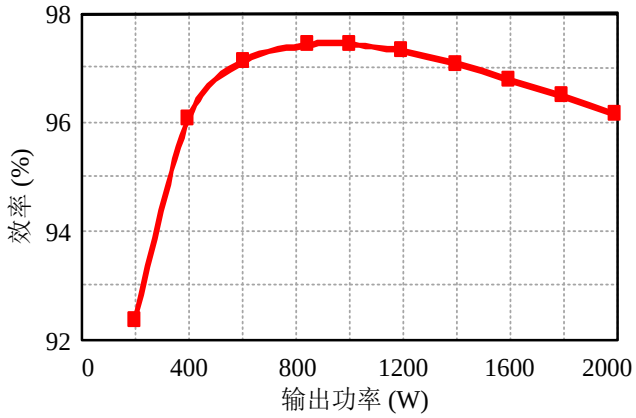


Figure 4.8 Efficiency curve as a function of load

Compared with traditional Si devices, the application of GaN devices is beneficial to improving the converter frequency and reducing the loss. The increase of switching frequency not only facilitates the miniaturization of the power supply system, but also can speed up the dynamic response of the closed-loop control system, which is of great significance to the PoL switching power supply. The reason is that the load rate of the PoL power supply changes very frequently. And it is often switched quickly between standby, full power and partial power conditions. In order to further improve the conversion efficiency of the power supply system, it is urgent to develop non-isolated converters with soft switching characteristics.

The 48-to-12-V isolated intermediate bus converter with GaN devices has a output power of 400 W, a switching frequency of 1.2 MHz and an overload efficiency over 96%.And its loss is 25% less than that of the converter with Si MOSFETs; the 48-to-12-V half-bridge current mode resonant converter has a maximum output power of 120 W, a switching frequency of 5 MHz and a full-load efficiency of 90%; The 19-16 V, 50 W Buck converter fabricated with GaN power devices of E company has a switching frequency of 8MHz and a efficiency of 89%. The server power supply (LLC + Buck) using 600 V GaN devices of T company has a operating frequency of 500 kHz and an output of 50 V/ 4 A, and its conversion efficiency is 15% higher than that of the device using Si MOSFETs.

4.2.3Power adapters

Small portable electronic equipments and power supply voltage conversion devices for electronic appliances are commonly used in mobile phones, liquid crystal displays, notebook computers and other small electronic products. Its function is to convert 220V to a stable working voltage of about 5-20 V for these electronic products. In reality, most of the power adapters around us are switching power supplies. At present, about 1.8 billion mobile phones and 150-170 million portable notebook computers are produced in the world each year. All these electronic devices require small and lightweight portable adapters. The average mobile phone charger

power is concentrated at 10-15 W, and the charger power of laptop is concentrated at 65-80 W. The need for miniaturization of adapters is a major driving force for GaN devices in this application.

The performance advantages of GaN electronic devices make them ideal for fabricating small, high-efficiency adapter power supplies. Most traditional notebook power adapters adopt a hard-switching mode flyback converter circuit topology. This type of converter operates in hard-switching condition. Not only the switching loss of power devices is very large, but also the leakage inductance energy of transformer cannot be recovered, resulting in a low system conversion efficiency, thus restricting the miniaturization and high frequency of the power adapter. Later, a soft-switching converter with quasi-resonant mode was proposed. Such a converter can effectively recover the leakage inductance energy and improve the conversion efficiency of the power supply system, but a snubber circuit still needed. Since the loss of the snubber circuit is proportional to the switching frequency, the actual switching frequency of the converter is not higher than 125 kHz.

In order to further improve the operating frequency and conversion efficiency of the flyback converter, the active clamped flyback converter (ACF) topology has been proposed (Figure 4.9 [16]). This circuit topology not only enables leakage energy recovery, but also need no snubber circuit. Under the critical mode of operation, the converter can also achieve zero current turnoff of the synchronous rectification circuit.

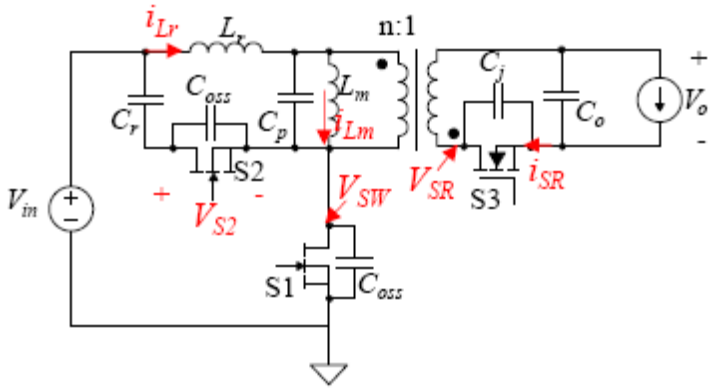


Figure 4.9 Circuit diagram of the active clamped flyback converter

Currently, Navitas and TI have jointly developed the 65W series chargers using GaN power devices. The maximum switching frequency of this power supply system is 446kHz, the maximum conversion efficiency is higher than 94%, and the average efficiency at 4 points (25%, 50%, 75% and 100%) is greater than 92%, resulting in a high power density of 39.3 W/in3. The future development trend of miniaturization is half-bridge + driver integration. And it is even possible to adopt SIP system-level packaging technology.

4.2.4 Power PFC applications

In addition to mobile phone chargers, some low-power household appliances,

lighting and display power supplies also have a strong demand for miniaturization and high efficiency. The power factor (PF) is a parameter used to measure the power efficiency of electric equipments, and alow PF represents alow power efficiency. There are capacitive and inductive devices in power and consumer equipments, which lead to the phase difference between current and voltage, resulting in the loss of the switching power. According to the regulations, the PFC function is required when the voltage of the power supply is above 75W.Since May 2002, China has regulated the procurement of electronic equipment by government agencies, and regards power factor correction (PFC) as a standard function of electronic equipments.

Since its entry into force in 2007, Energy Star 80 PLUS Technical Specification for Efficiency Assessment has increased the efficiency level of AC/DC rectifiers from gold to higher platinum, and continues to increase to titanium. However, efficiency improvement are slowing down due to the performance limitation of MOSFETs and significant design challenges associated with titanium-level efficiency requirements. In order to achieve 96% titanium-level peak efficiency, the budget efficiency of power factor correction (PFC) circuit efficiency should reach 98.5% and above for high-voltage circuits, and should not be lower than 96.4% for low-voltage circuits.

The low RDSON, low parasitic capacitance and fast switching property of GaN FETs enable them to be used to develop efficient PFC circuits. In addition, utilizing the characteristics of GaN devices, it is possible to use fewer devices than Si devices to achieve an efficiency above 98% with a totem polebridgeless topology.

Figure 4.10 shows a PFC circuit developed by TI using GaN devices. Figure 4.11 shows that it achieves 99% efficiency at 1 kW.

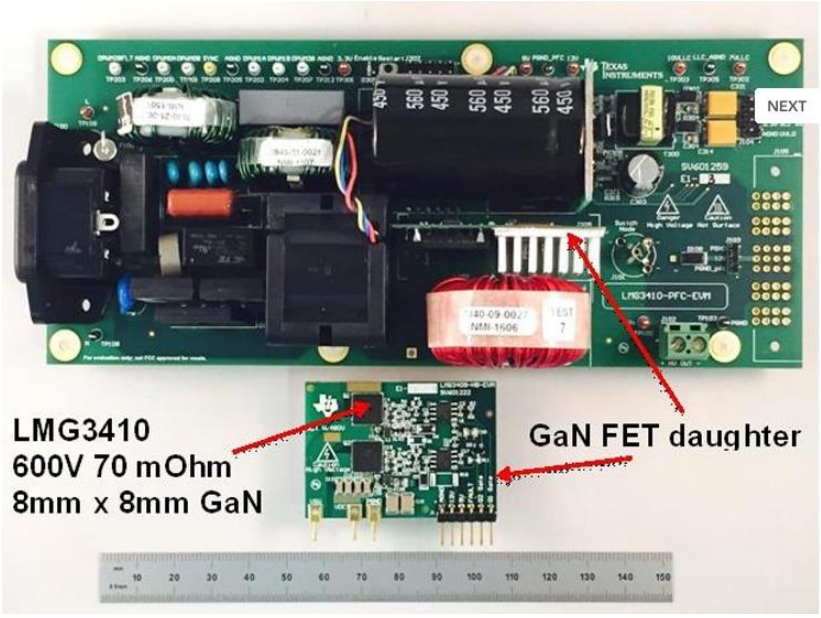


Figure 4.10 TI's power master based on GaN device PFC (source: TI website)

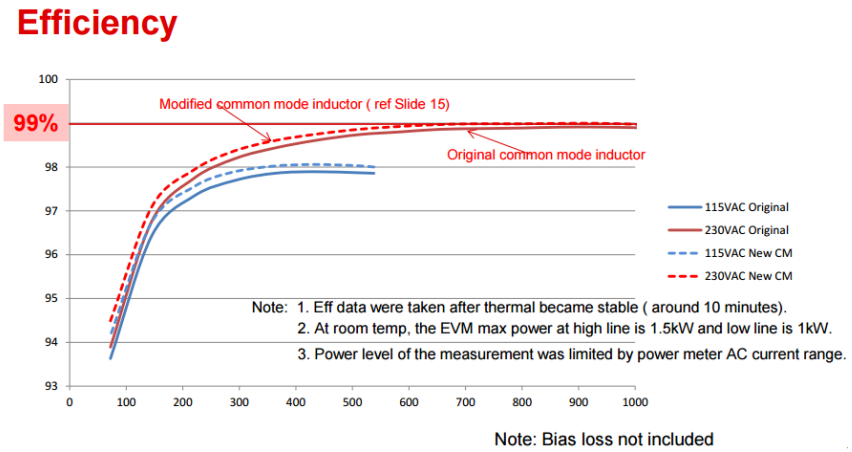


Figure 4.11 TI's PFC efficiency changes with power based on GaN devices (source: TI website)

4.2.5 High frequency lidar applications

In recent years, the demand for lidar has increased rapidly due to the rise and popularity of unmanned vehicles. Initially, lidar was used for ranging, measuring wind speed, air disturbances and so on. With the promotion of demand for unmanned vehicles, the demand for 3D imaging is growing rapidly.

By emitting high-frequency laser pulses, and comparing the collected reflected laser signals with the reference signal, the lidar can obtain a lot of information of the laser pulse scanning point, such as surface materials, distance, motion and so on. As the core device of a laser drive, high-frequency power devices should have fast, low parasitic capacitance and large pulse power.

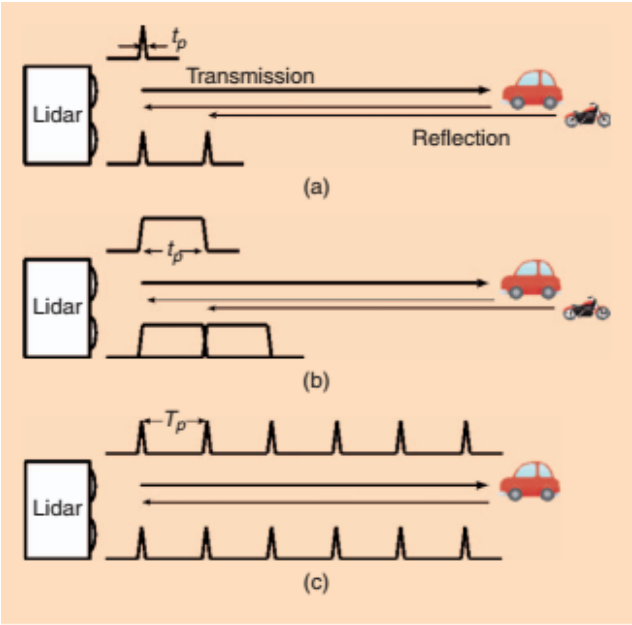


Figure 4.12 Influence of lidar pulse width on distance measurement resolution

In Figure 4.12, A) shorter pulses facilitate the distinguish of two consecutive

reflected pulses and improve the resolution. B) Wide pulses are more likely to overlap and make it difficult to distinguish targets. C) Narrow pulses make the different pulses in the high frequency pulse sequence easier to resolve, thereby increasing the resolution.

The driver based on the GaN device can effectively improve the quality factor and greatly increase the switching speed. The shorter pulse rising and falling edges of GaN devices, allow the emitting of shorter pulses and higher scanning frequency to achieve 3D imaging with higher resolution and faster measurement speed.

The resolution can be greatly improved by lidar. The figure below compares the results of lidar scanning based on Si MOFET and GaNtransistor driver. It is obvious that the lidar has a higher scanning resolution.

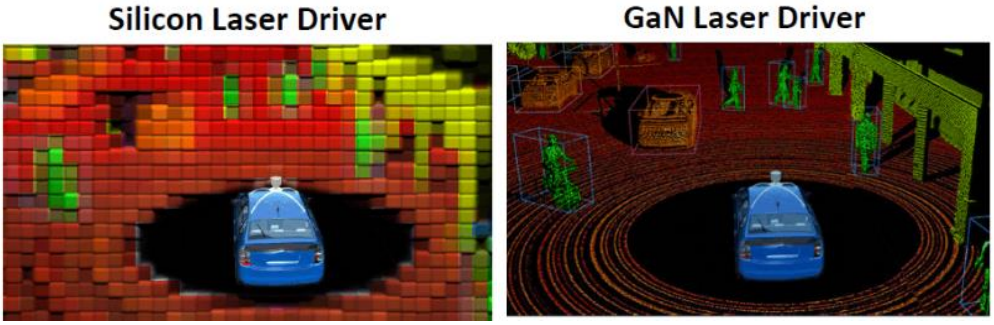


Figure 4.13 Comparison of lidar imaging resolution driven by Si and GaN devices (source: US EPC Corporation)

The EPC Corporation takes the lead in the lidar GaN drive market. Its 15-100V device has a pulse width less than 5 nanoseconds on the new generation of multi-channel lidar. Velodyne, in collaboration with EPC, has begun using GaN devices to drive high-resolution lidars on 64 channel radars.

With the gradual development and future application of automotive and auxiliary driving, high-resolution lidar will gain an increasing broad market share. Gradually there will be more mainstream lidar companies using GaN as the laser driver to improve the resolution of the lidar.

4.2.6 Signal envelope tracking

In modern mobile communication systems, in order to improve the data transmission rate and utilize spectrum resources more efficiently, modulation methods with higher spectrum utilization, such as quadrature phase shift keying and quadrature amplitude modulation, are usually used. This type of modulation will lead the envelope of the radio frequency (RF) input signal to change over time and has a large peak-to-average power ratio (PAPR), as shown in Figure 4.14 [17]. At this time, in order to ensure the linearity of the RF output signal, a linear power amplifier (LPA), such as a class A and class AB linear amplifier, is required to amplify the RF input signal. However, the LPA using the constant voltage power supply mode is less efficient when amplifying the RF signal with a large PAPR, resulting in huge energy waste. For example, when the PAPR of the RF signal is 5 dB, the efficiency of the

Class A amplifier is only 10%. Therefore, it is imperative to improve the efficiency of LPA.

Envelope tracking (ET) technology can greatly improve the efficiency of LPA. The basic idea is to dynamically adjust the LPA supply voltage according to the envelope amplitude of the RF input signal, so that the LPA always maintains high efficiency, as shown in Figure 4.15 [17].

Figure 4.16 shows the principle block diagram of ET technology [17]. The envelope of the RF input signal is detected by the envelope detector and used as a reference signal for the DC/DC converter. The output voltage of the DC/DC converter is used as the supply voltage for the LPA. The delay link is used to match the delay of the envelope path and the RF path. The DC/DC converter is the ET power supply, which is the core of the ET system. In order to achieve a high system efficiency, the ET power supply needs to have a high efficiency first. And secondly, the ET power supply needs to have a relatively wide tracking bandwidth to ensure the tracking of the RF input signal envelope, thereby enabling the LPA to achieve higher efficiency. With the development of mobile communication, the envelope bandwidth of the RF input signal is gradually increasing. In the 4G mobile communication system, the envelope bandwidth has reached 20MHz. How to efficiently track the envelope signal with large swing and high speed exchange poses a great challenge for the designof ET power supply.

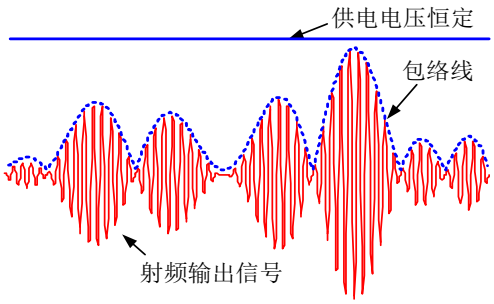


Figure 4.14 Typical waveform for constant voltage supply

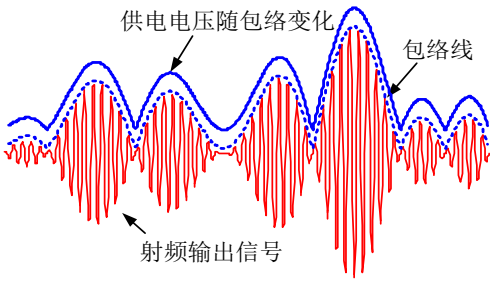


Figure 4.15 Typical waveform of the envelope following the power supply

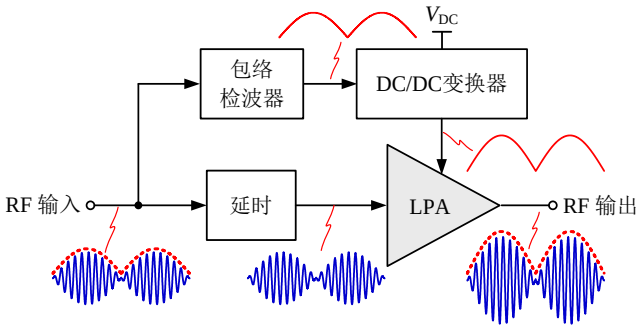


Figure 4.16 Block diagram of the technology

Due to the high efficiency of switching converters, ET power supplies typically include switching converters. The tracking bandwidth of a switching converter is usually much lower than its switching frequency. Therefore, the required switching frequency will be very high to achieve such a high tracking bandwidth, and the huge switching loss caused by conventional Si devices will seriously reduce the efficiency of the switching converter. Compared with Si MOSFETs, GaN FETs have high carrier mobility, low on-resistance and low parasitic capacitance, which make them suitable for applications with high operating frequencies. Therefore, the performance of the switching converter in the ET power supply can be greatly improved by using GaN FETs.

At present, the application of GaN in signal envelope tracking is relatively mature.

4.2.7 Wireless charging

In the past two years, with the promotion of Apple's iPhone, low-power wireless charging has gradually been accepted by the public as a daily application. The standards and solutions for wireless charging have evolved into two major alliances and charging standards, the Wireless Power Consortium (WPC) and the Airfuel Alliance. At present, the wireless charging used by iPhone is the Qi standard of the WPC Alliance, which adopts 100-205 kHz charging frequency and magnetic induction technology. As the distance increases, the efficiency drops dramatically.

In addition, the Wireless Charging Alliance A4WP (now part of the Airfuel Alliance) has released rezence, which uses electromagnetic resonant charging technology to enable wireless charging over long distances (cm-m). It contains a high frequency of 6.78MHz charging solution. The current 6.78MHz wireless charging scheme is an good upgrade for high frequency GaN device applications. The high frequency and high power characteristics of GaN devices make them ideal for 6.78MHz wireless charging applications.

Conventional Si power devices typically operate at frequencies of a few hundred kHz and do not meet the requirements for use. For example, the wireless charging power supply based on Class E technology requires not only a switching frequency of the power device of 6.78 MHz, but also a withstand voltage of up to 200V. The future development direction is still to continuously improve the system's operation

frequency. Take the medium and small power 6.78MHz wireless charging system as an example, the higher the operating frequency, the smaller the size of the power module.

In the future, with the rise of various power facilities including wireless charging of high-power electric vehicles, wireless charging will gradually increase rapidly.

4.2.8 On-board charging

With the development of electric vehicles, power electronic devices are widely used in the automotive field. Plug-in electric vehicles are growing rapidly at present. In the field of on-board chargers, there are companies doing development work currently.

On-board chargers with GaN devices can effectively reduce the number of power devices used, and simplify the circuit.

With GaN power devices, the number of power devices in the OBC system is expected to be reduced from 76 (with Si devices including transistors and diodes) to 24. The operating frequency is increased from below 100KHz with Si devices to 300K-1MHz with GaN devices. Thus, the system volume can be reduced by 20-30%. And the efficiency is expected to increase from 93% to 95%.

4.3 Discussion and countermeasures of some necessary conditions for application implementation.

4.3.1 New requirements of new applications for GaN devices

With the in-depth study of GaN devices, the conditions for applying GaN devices to industrial products are gradually approaching maturity. At this stage, the introduction of the characteristic advantages of GaN devices into industrial products has become an important trend in the development of new devices, and this will put forward some new requirements for GaN devices.

As mentioned earlier, normally-off devices are the requirements of power application engineers and can easily meet the criteria for fail-safe. A current approach for normally-off GaN devices is achieved by Cascode, cascading a Si MOSFET to the GaN normally-on device. However, the advantage of high frequency of GaN cannot be brought into full play through this method. In addition, the normally-off GaN FET with a junction gate structure is commonly used on the market. Insulated gate GaN MISFETs are also under development. There is a need in the future for easy-to-use, standardized GaN normally-off devices. This requires continuous improvement and maturity during device development.

In large-scale industrial applications, first it is necessary to ensure the stability and

consistency of power devices, which requires semiconductor materials and device manufacturers to have mature production conditions and equipment as a guarantee. Second, industrial applications place higher demands on device reliability. Study of reliability requires a large amount of experimental data as support and requires high time costs. The testing and research of new device reliability is in progress, but it is not perfect at present. There are no reliability test standards for GaN devices. And we realize that the JEDEC organization is developing test standards for the reliability of GaN devices and it is expected to be completed by 2018.When the reliability of GaN devices is verified and accepted by customers, large-scale industrial applications are just around the corner. On the other hand, in practical applications, the convenience of product assembly is also very important, which requires the search for a suitable package form, which can improve the convenience of its use while exerting the excellent characteristics of GaN devices.

In terms of device reliability test standards and tests, technically the reliability issues should include the following:

a) Basic research on failure mechanism

b) Accelerated test method

c) System reliability prediction and fault diagnosis estimation software

d) Multi physical field composite load detection equipment

e) Reliability database based on big data and cloud

f) Establishment of standard

In terms of packaging form and standardization, the main technical points that can be considered at present:

a) Welding and sintering

b) Double-sided heat dissipation

c) Liquid cooling structure

For high power packaging, there are two commonly used forms: one is traditional chip +direct bonded copper (DBC)+ substrate. This type of package is relatively mature and simple, and the cost is low. However, there are two major disadvantages: First, due to the difference in the coefficient of thermal expansion (CTE) between the DBC and the substrate, the solder joints connecting them will generate fatigue cracks under high temperature cycling, eventually leading to the failure; second, because this type of package is one-way heat dissipation with low efficiency, there will be a great challenge when doing thermal management in package design. The other is a full-crimping module, that is, a plurality of chip positioning devices are arranged in the module, and then the molybdenum sheets (with a thermal expansion coefficient very similar to the chip) and the chip are sequentially placed into the positioning device, and then crimped. This crimping method can achieve double-sided heat dissipation, and the connection between the chip and the molybdenum sheet usually uses a high-melting nano-silver paste or a silver film, thereby having excellent heat dissipation and high reliability. Especially for high power applications, the advantages are more obvious.

4.3.2 Problem of matching components

4.3.2.1 Problems of magnetic components

With the increase of working frequency, the technology of magnetic transformer and power filter should be improved accordingly. In addition, the problem of conductive EMI electromagnetic interference caused by distributed capacitance is becoming more and more serious.

The operating frequency of the core is low.

The operation frequencies of most magnetic materials are below 500 kHz. If the switching frequency is too high, not only will the core loss increase sharply, but the inductance will show strong instability and nonlinearity.

Plane transformer winding process needs to be improved.

At high frequencies, the skin effect and proximity of the coil are very obvious, so the alignment and shielding of the wound wires need to be considered in particular.

The demand for magnetic integration is urgent.

Magnetic components account for a larger proportion of the GaN power system. Therefore, in order to reduce the size of the power module, magnetic integration needs to be considered. Corresponding research and development is in progress.

4.3.2.2 Challenges of gate drivers and dedicated analog control chips

In practical applications, in order to match the high frequency operation and driving voltage of GaN devices, it is necessary to redesign a special GaN gate driving chip. At present, TI has introduced many products in this field. And the current main problems are:

Integrated driver chips are not enough

The gate withstand voltage of GaN devices is only 7V, which is much lower than other Si devices; the maximum switching frequency can be more than 2MHz, and the rise/fall time is less than 1ns. There are only a few available gate drivers available on the market today.

Application of high-side driver is difficult

In a half-bridge/full-bridge circuit topology, the driving pulse energy of the high-side device requires a bootstrap capacitor supply. In high-frequency switching applications, the energy extraction of the bootstrap capacitor and its reliability can be highly uncertain.

Cooling problem

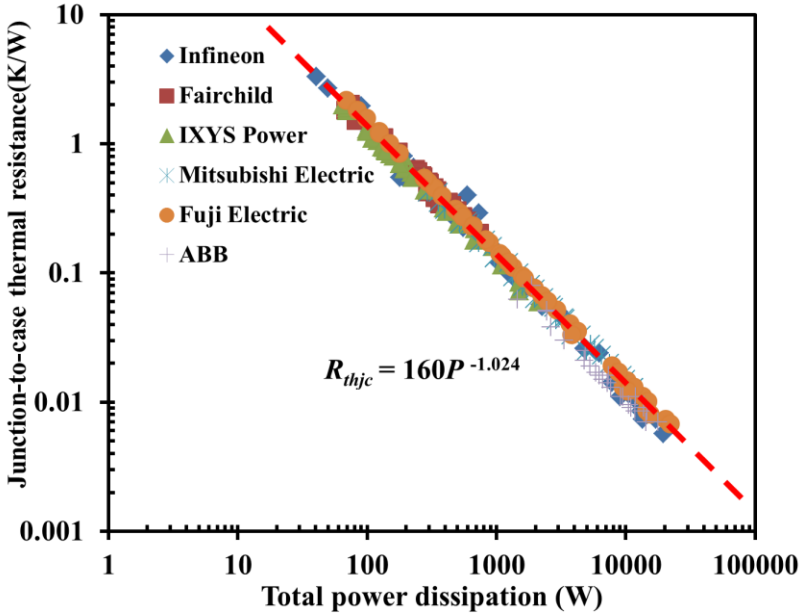
When the operating frequency is increased, the amount of heat generated by the gate driver is sharply increased.

Totem PFC technology requires GaN power devices to achieve 99% efficiency and meet the US Energy Star standards. However, due to the lack of a dedicated

analog integrated control chip, the application of this technology in small and medium power supply systems is greatly limited. In the future, we expect more dedicated analog integrated control chips suitable for GaN devices and the development of GaN applications can be greatly advanced.

4.3.2.3 EMI electromagnetic interference

Due to the high operating frequency of GaN devices, the switching speed of GaN devices is faster, and the di/dt and dv/dt are larger at on/off instants, which will lead to the EMI pulse with wider spectrum range in the power supply system. In addition, the threshold voltage of GaN devices is much lower than that of Si devices. This leads to the larger



sensitivity of the electrical EMS magnetic interference. In the design of application, more consideration should be given to EMI.

4.3.3 Thermal management

Although the power efficiency of GaN devices has been improved, the heat dissipation ability and thermal management of the system still need further research because of the increased power density of GaN devices.

In terms of packaging, the thermal resistance development trend of DBC-based silicon devices is shown in Figure 4.17 [18]. From the thermal perspective, the development trend of GaN and SiC should be basically the same.

Fig. 4.17 Development trend of the thermal resistance of DBC-based silicon devices

With the double-sided heat dissipation, the thermal resistance will be reduced by half. However, the corresponding heat dissipation structure and the assembly will change. In practical applications, because of the increased power density of GaN devices, compared with Si devices, GaN devices with the same power level become smaller and smaller, and their thermal resistance increases accordingly, which puts forward higher requirements for the cooling system of industrial products. At present, the main solutions to this problem are double-sided cooling and liquid cooling. With double-sided heat dissipation, the thermal resistance will be reduced by half. However, the corresponding heat dissipation structure and the assembly will change, which puts forward new requirements for the structural design of industrial products. The heat dissipation of cooling system is better by using cooling liquid circulation. But the cost of maintenance and assembly are high. Full liquid cooling is a trend in the development of heat dissipation technology.

4.3.4 Evolution of topology

The application topology of GaN is still in the form of Si devices, without much change. In fact, compared with Si-based super junction MOSFET devices, the advantages of GaN devices under hard-switching conditions are not obvious. However, its performance advantage under soft-switching condition is very prominent. Based on this, the resonant circuit topology which can achieve soft-switching can better demonstrate the advantages of GaN devices. At the same time, the switching loss of the device increases gradually with the increase of the switching frequency, while the soft-switching technology can greatly reduce the switching loss and improve the conversion efficiency. However, the conventional circuit topology is still based on traditional PWM hard-switching mode. With the development and application of GaN devices becoming more and more mature, the evolution of the corresponding topology will become a new research hotspot in the future.

4.4 Prediction of evolution of main performance parameters

4.4.1 Efficiency

4.4.1.1 key points

- The challenges of realizing an efficient and stable GaN based power system are mainly as follows:

1. High switching frequency: GaN can work at higher frequency, reduce the volume and increase the power density. However, this leads to higher switching losses, higher requirements for magnetic components and increased electromagnetic interference (EMI).
2. Gate driving: Due to the high dead time, the low threshold voltage and the need for floating recommended driving voltage, GaN HFET requires dedicated gate drivers.
3. Parasitic inductance: GaN packaging and PCB circuits have strong parasitic inductance effects at high frequencies, which affects the power efficiency.

- There are several ways to reduce loss and increase efficiency：

1. Circuit topology: Usually a coupled or semi coupled (quasi-resonant) topology is used.
2. Soft-switching: High frequency soft-switching and synchronous rectification technology.
3. Precise dead time control can reduce the conduction loss and improve the efficiency under high frequency operation.
4. Passive device optimization. It is necessary to optimize the selection of suitable passive devices and the design of PCB boards.

At present, due to the immature development in these aspects, GaN has not yet maximized its advantages.

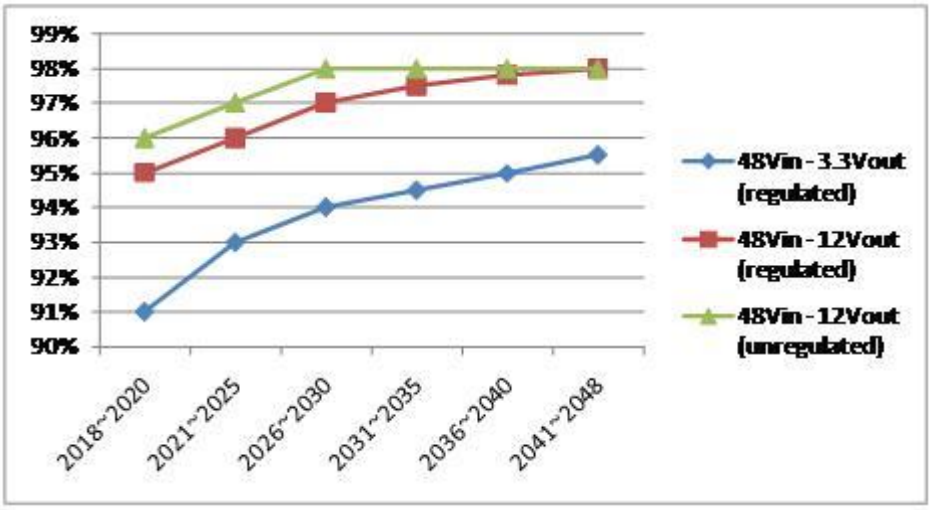
4.4.1.2 Efficiency prediction

Take the 48 V DC-DC application as an example. At present, the efficiency of such systems is 91% (48V-3.3 V). With applying the third generation semiconductor devices, the efficiency will gradually increase to more than 95% in the future. The prediction is shown in Figure 4.18.

Figure 4.18 Trends in conversion efficiency of DC-DC converters.

4.4.2 Evolution of power dimension and power density

In the future, various power supply systems, such as chargers, automotive charging piles, photovoltaic inverters and so on, need miniaturization, high efficiency and lightweight power systems. Lightweight and miniaturization are important considerations in many applications. High-speed switching frequency and low loss of GaN devices can effectively reduce the volume of inductor capacitors. At the same time, due to the low loss, high efficiency and high temperature resistance of GaN



devices, the requirement for heat dissipation and volume occupancy are further reduced. In summary, power systems based on GaN devices can provide higher power density.

Challenges of size reduction include the following points:

1. Heat dissipation;
2. EMI;
3. Inductor size.

These three problems can be solved by proper packaging and optimized topology.

4.4.2.1. Ways to reduce size

1. Reduce device size by 3D packaging and other packaging methods.
2. Miniaturized passive devices. Especially through the next generation of ferrite and planer current transformers, the size of inductors can be effectively reduced.
3. Optimize topology, such as LCLC developed from optimized LLC.
4. Introduce synchronous rectification and soft-switching technology to reduce the pressure of heat dissipation.

4.4.2.2 Technical difficulties

- Packaging technology

For GaN applications, there will be great demand for packaging in the future. The packaging structure with low cost, high integration, low parasitic parameters and excellent heat dissipation capability is in great demand. At present, the common TO series packaging structure and QFN packaging can not take full performance advantages of GaN devices. 3D packaging, embedded and higher integrated packaging are the possible directions in the future.

- Optimization of topological structure

The application of GaN requires a new topology to reduce the influence of electromagnetic interference, further improve the circuit frequency and reduce the size of power supply.

- Passive device size reduction

The size of the power supply system is more determined by the inductor, capacitor and other passive devices, and the heat dissipation part. Choosing proper capacitors and new core materials of the inductor will be conducive to reducing the volume of passive devices. At present, good magnetic materials need to be further developed under 500 KHz-1 MHz operating frequency.

4.4.2.3 Prediction of power density in the future

Based on the above judgement, we also give the future evolution of the power density for GaN power device applications.

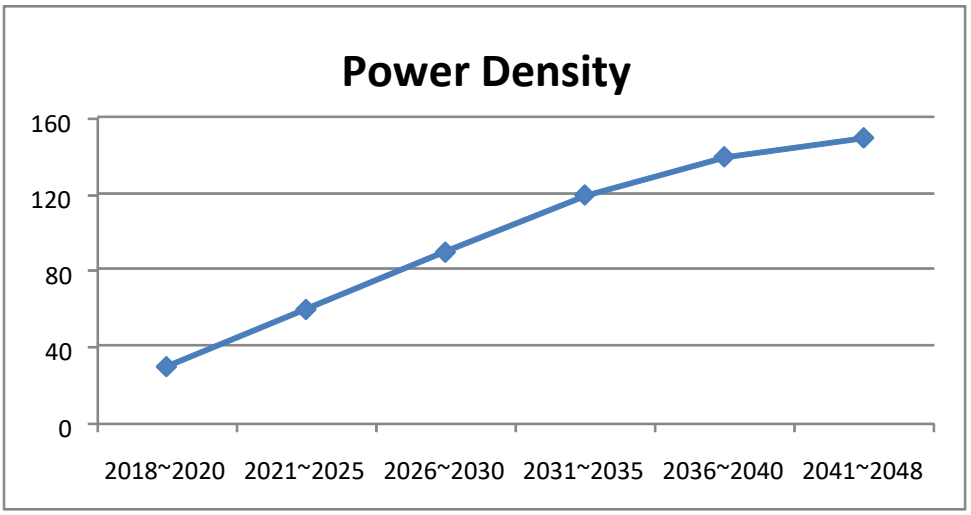


Fig. 4.19 Trend development of DC-DC converter power density (W/cm3)

4.4.3 Cost

At present, the price of GaN devices is still relatively high, which is 4-5 times that of Si devices at the same voltage level, which seriously limits the application of GaN. Taking the 65 W computer adapter (without PFC function) as an example, GaN devices account for 70% of the total BOM(bill of material) cost in the BOM cost.

Currently, the cost of GaN devices is mainly derived from the epitaxy. Here the cost of raw materials and energy is estimated in terms of the GaN wafer on 6-inch silicon. The price of 6-inch silicon wafers is $30-35, the cost of epitaxy is about $300 per wafer, and the cost of device processing is close to $150. Thus, the cost of raw materials, energy and technology is about $500. And epitaxy occupies nearly 2/3 of the cost.

At the end of 2017, the price of each 6-inchwafer device was close to $1500, including labor costs, sales costs, research and development investment and so on. The price still has a relatively large room for decline.

Table 4.2 Price forecast (equivalent to current monetary price)

Year	Epitaxy cost ($)	Device wafer cost ($)	Device price ($)(650 V, 20 A)
2018	300	500	4
2023	200	380	2
2028	150	310	1
2033	130	280	0.8
2038	110	260	0.6
2043	100	240	0.5

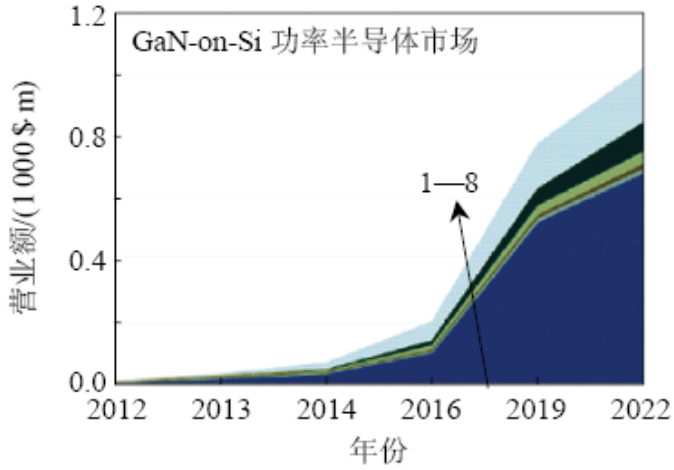
Analyzing from the perspective of cost, there is still great potential to develop the epitaxial part in the future, thus reducing the total cost of GaN devices.

4.5 Risk and related issues

4.5.1 Market and price

Compared with Si materials, GaN has many excellent properties. At first, the substrate material of GaN has to be sapphire or SiC wafer, thus the development of GaN has been limited. Later, with the powerful promotion of LED lighting application market, the development of GaN heterojunction epitaxy technology has made a qualitative leap, which opens up a broad way for GaN materials and devices to reduce costs substantially. Then GaN power electronic devices are also popular in the industry.

The market size prediction of Si-based GaN power devices is shown in Figure 4.20. After 2016, with the gradual maturity of GaN-on-Si technology, the demand for GaN power electronic devices is entering a period of rapid growth.



1-switching power supply; 2-uninterruptible power supply; 3-hybrid and electric vehicle; 4-industrial motor drive;5-photovoltaic inverter; 6-wind turbine; 7-traction; 8-other applications.

Figure 4.20 Forecast of GaN-on-Si power electronics market (source: IHS)

At present, the price of GaN devices is still very high, which is about 4-5 times that of Si devices at the same voltage and current level. But IHS gave a positive prediction of the GaN device prospects. The reason is that the production cost of GaN devices is decreasing rapidly. It is estimated that the price of GaN products will be almost the same as that of traditional Si devices by 2019. This is conducive to the promotion of GaN products.

However, the famous Yole is still optimistic about Si-based devices. GaN devices are gradually used in high-frequency switching applications in the low and medium voltage range of 100-200 V, but the market share is still very small. GaN devices will gradually enter the 600 V high-frequency market, but most of them are limited to specific markets, such as on-board chargers for electric vehicles and power supply units in data centers. Due to the reliability and cost performance of Si power

MOSFETs, the main market will continue to use Si power MOSFET for a certain period.

Generally speaking, GaN devices represent a new direction for the development of power electronic devices. At present, GaN devices are mainly fabricated on heterojunction materials with transverse structure. It is difficult for GaN devices to withstand voltage more than 1 kV. Therefore, GaN devices will compete with Si-based power electronic devices in low voltage applications where the requirements are more stringent. Because of the excellent characteristics, GaN devices may be mainly used in consumer electronics, computer/server power supplies and other applications under 900 V.

4.5.2 Problems

In the past five years, GaN power devices have been developing rapidly, and many start-ups have emerged. Nevertheless, GaN technology needs further maturation, and the accumulation is not complete. There are still many technical problems to be solved.

4.5.2.1 Technical problems of GaN devices

GaN power devices have a long way to go for large-scale applications. The main technical problems are as follows:

- Reliability problem. Compared with Si power devices, the reliability and stability of GaN power devices are still lagging behind. Despite some research reports ofthe law of device degradation, failure mechanism and mode, and methods to enhance reliability, it is far from meeting the requirements for large-scale practical applications.
- Epitaxial growth technology. GaN epitaxy on large diameter Si substrates still faces many problems, such as the thermal and lattice mismatch between Si substrates and GaN materials, and the diffusion of Si atoms in GaN.
- Device breakdown voltage. Theoretically, under the same breakdown voltage, the on-resistance of GaN power devices is lower than that of Si and SiC power devices, but its performance is far from the theoretical value. It is found that the main reason is that the through the longitudinal penetrated GaN buffer layer, a leakage current is formed between the source and drain along the interface of silicon substrate and the GaN buffer layer.
- Implementation methods of enhanced device. Devices based on AlGaN/GaN structure are depleted (normally-on) devices. Whereas, enhanced (normally-off) power devices with positive threshold voltage can ensure the safety of power electronic systems, reduce system costs and complexity, and so on. Therefore, They are the preferred devices in power systems.
- Current collapse suppression technology. There are four main methods to

restrain current collapse: surface passivation, field plate, falling layer(冒层) and barrier layer doping. The four methods have their advantages and disadvantages, and a standardized process has not been formed yet.

- Low cost process technology. The key to develop GaN power device manufacturing process compatible with existing Si manufacturing process is to develop gold-free process, which is an important approach to reduce cost and realize mass production and large-scale commercial application.
- Power integration technology. Forming independent and complete modules, including GaN power core devices, device drivers, protection circuits and peripheral passive devices, directly facing the terminal application is the development direction of GaN power devices. This will help GaN devices to achieve high performance, high work safety, high speed and high temperature tolerance that traditional Si power chip technology can not achieve.

4.5.2.2 Bottlenecks of GaN application and power technology

- High-precision modeling method of wide-bandgap switching devices: The inherent switching and output characteristics of wide-bandgap switching devices will be affected by external factors, so deriving accurate mathematical model of output characteristics of wide-bandgap switching devices under the condition of high temperature, high frequency and harsh working environment is the main technical bottleneck.
- New topology by multi-objective optimization: Simple replacement of devices is far from giving full play to the performance of wide-bandgap switching devices. In the development of new topology, the complexity of strategies, overall efficiency, power density, power quality and other objectives need to be considered in a compromise. It is the main technical bottleneck to propose optimal topology schemes for multiple objectives.
- Compact design method for power electronic devices: In order to achieve compact design, the switching frequency can be increased and the volume of passive devices, filters and transformers can be reduced. On the other hand, when the switching power frequency is high, high requirements will be placed on the magnetic components. Therefore, for the compact design, the switching frequency, the size of power electronics, and the relationship between magnetic components need to be considered to achieve coordination and optimization.
- Optimized control method for power electronic devices: The new power electronic topology will lead to different positions and quantities of switching devices and diodes. And the split inductor, split capacitor filter and high frequency transformer are introduced. In order to ensure the high performance of the system, the control and modulation strategy of the new device is the main technical bottleneck.
- Integration of AC/ DC microgrid converters using wide-bandgap devices: In

order to develop miniaturized, lightweight and high-power-density power electronic devices, high precision and high reliability integration of electrical components is the main technology bottlenecks based on the full consideration of heat dissipation, anti-electromagnetic interference and reducing parasitic parameters.

- Exploring new topology and integration: It is well known that every topology change of power converters is closely related to the renewal of devices, and the emergence of a new generation of semiconductor devices may promote the birth of a new generation of topology. For example, boost transformers and inverters are often used in new energy vehicles to control the energy flow between the motor and the battery, which is relatively costly and bulky. In recent years, researchers have been trying to reduce hardware requirements by using matrix converters, Z-source converters, unconventional current sources and other topologies. The excellent characteristics of the third generation semiconductor devices can take advantages of the new topology to a certain extent, reducing the volume and weight of passive devices, and the overall cost of the controller.
- Packaging for high temperature operation: GaN devices can work at high temperatures above 200 °C. The power module also includes substrates, solders, insulation gels and other parts. At the present stage, these parts are only suitable for Si chips to operate at 125-150 °C, and cannot support the chip running at high temperature. It is necessary to develop power modules that are suitable for various occasions with a temperature of 200 °C and higher.
- Electromagnetic compatibility and high frequency magnetic components design: The high switching frequency of GaN will increase the electromagnetic interference of the equipment. In order to effectively improve the electromagnetic interference performance of the facility, it is necessary to study the generation mechanism and suppression methods of electromagnetic interference caused by the third generation semiconductor devices. In addition, there are many basic problems to be studied for high frequency magnetic components. With the increase of switching frequency, the iron loss of the magnetic material of the reactor will increase, which will lead to the decrease of the efficiency of the power converter. New magnetic material and winding process must be used.

4.5.3 Risk control proposal

GaN power device manufacturers should arrange power module technology in advance. According to the authority IHS, sales of GaN power module are expected to account for about 25% of the total sales. At present, device manufacturers should also deeply arrange the GaN device application markets, such as wireless charging, aerospace and military, helping system development companies solve the technical

problems encountered in device application and testing.

In the initial stage, we suggest that GaN power devices should focus on the application fields of medium and low voltage, medium and small power supplies under 650 V. Starting from the applications with technical advantages, we can accumulate the experience of understanding, improving and applying the device performance. We will find some killer applications to expand the application of GaN devices. The future will be gradually expanded in other fields.

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